

GA-AB350M-GAMING 3

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[illegible]

Model Name:GA-AB350M-GAMING 3

Component value change history

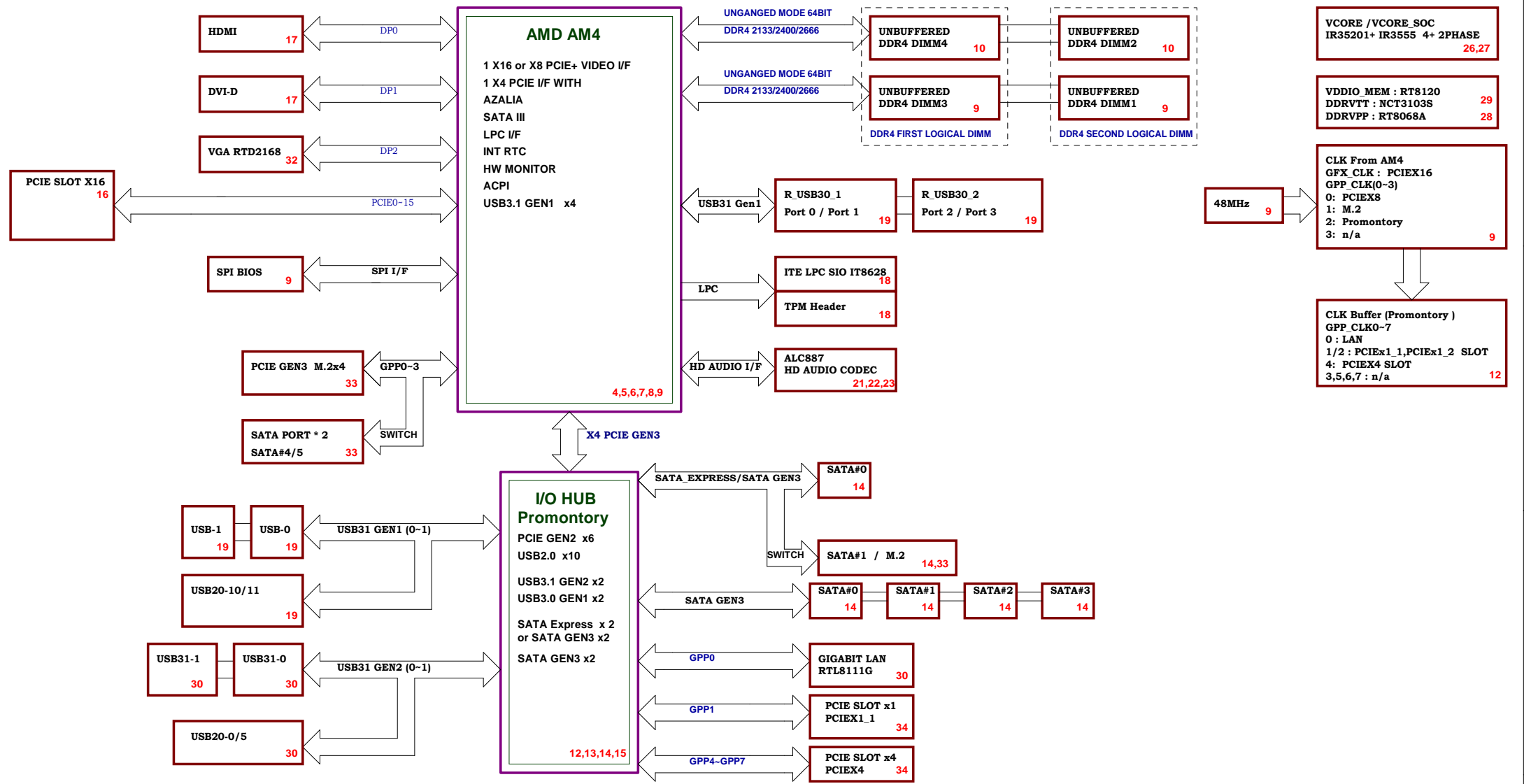
Version: 1.0

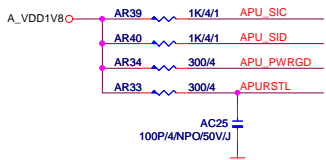
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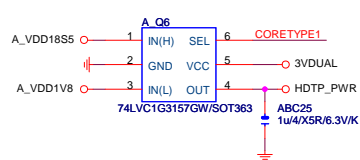
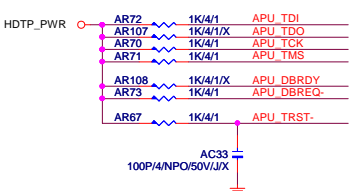
Circuit or PCB layout change for next version

[illegible]





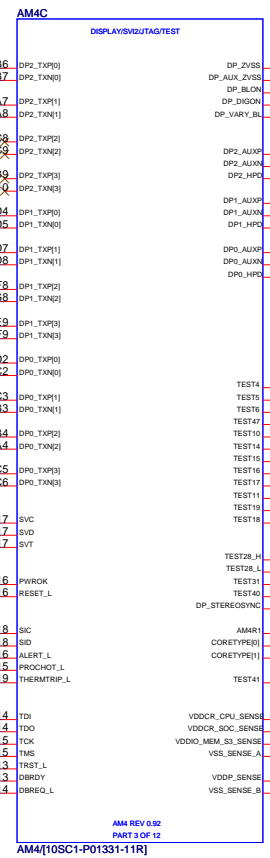
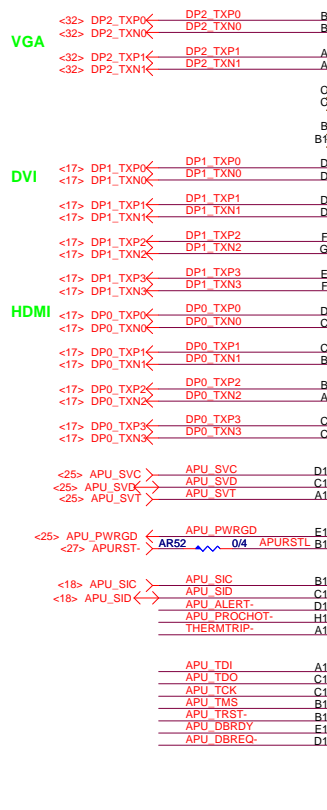
SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



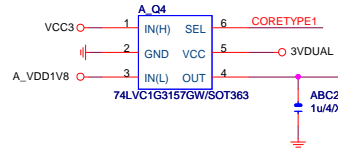
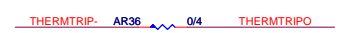
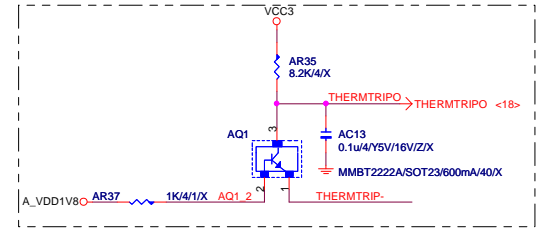
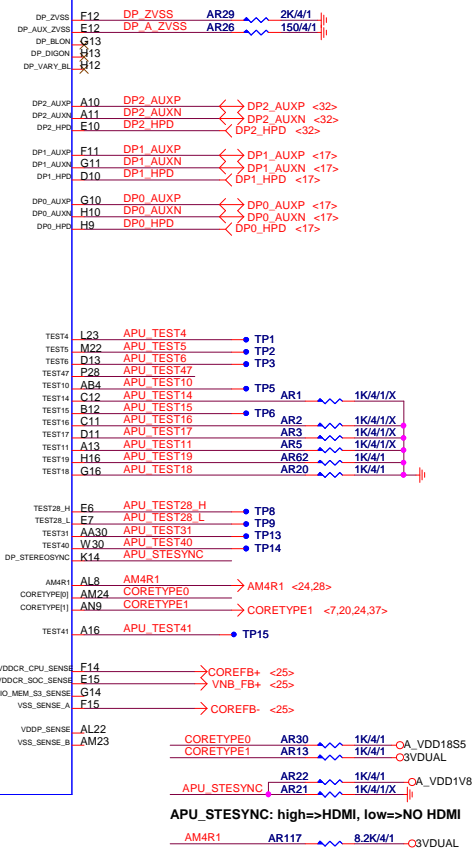
VGA

DVI

HDMI



Placed within 1500 mils from APU



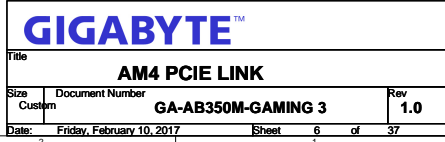
CORETYPE 1	CORETYPE 0	Family / Model	Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh		TYPE 0
0 ST	1	Reserved		TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh		TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh		TYPE 3

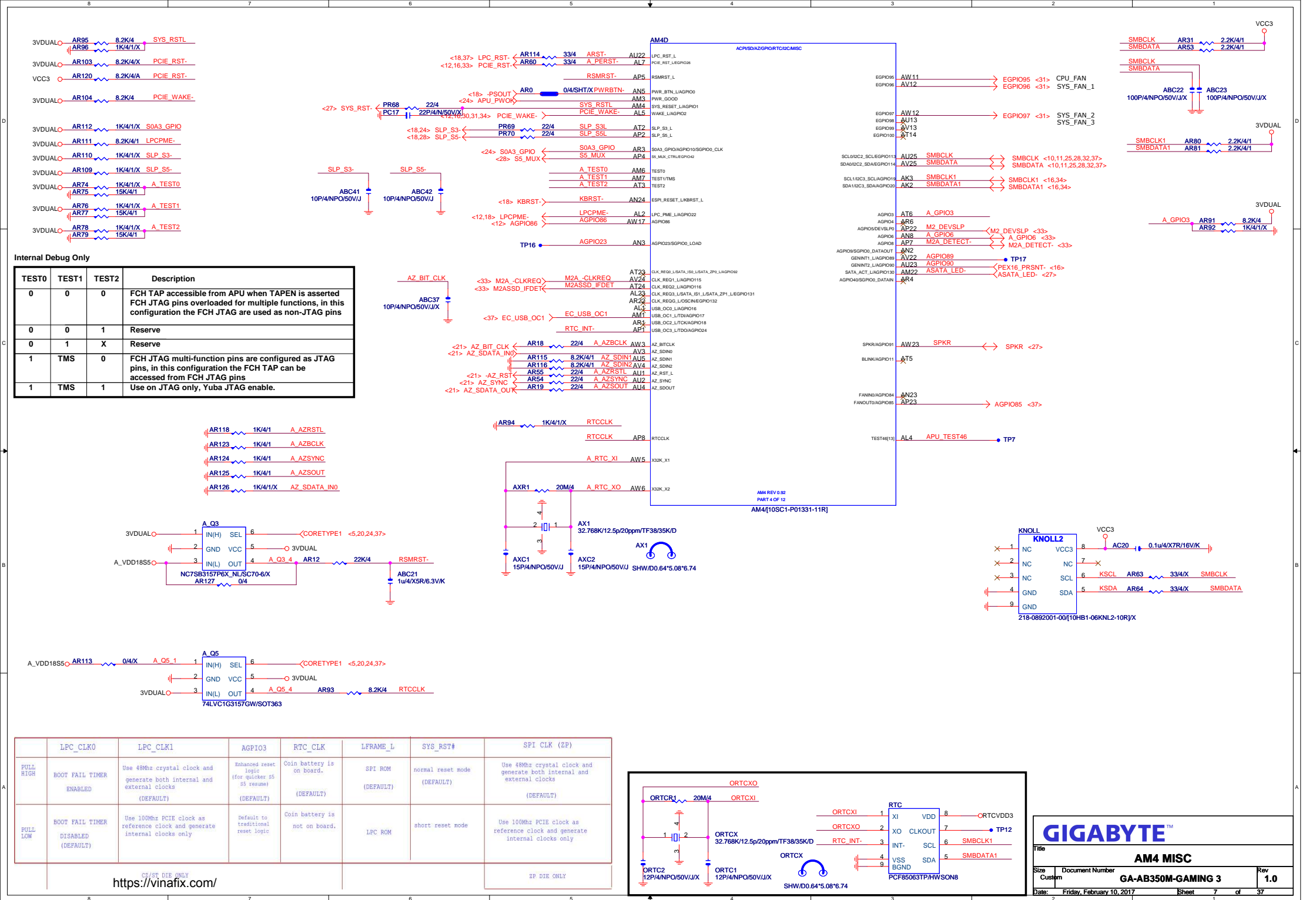
GIGABYTE™

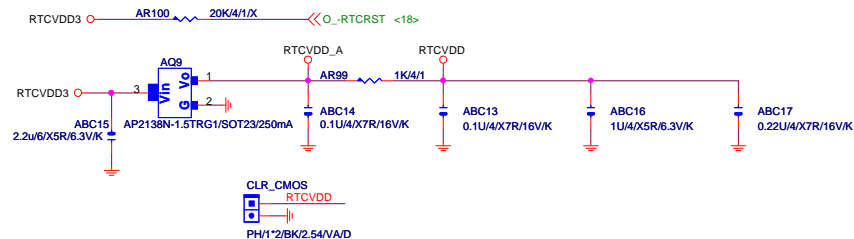
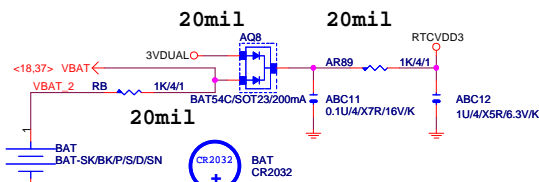
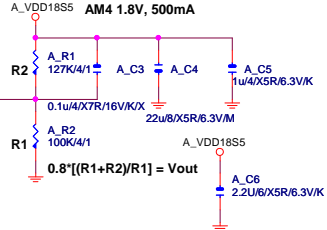
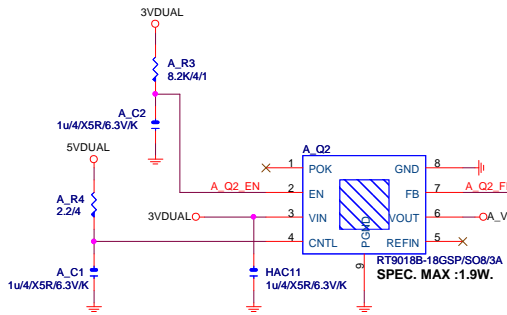
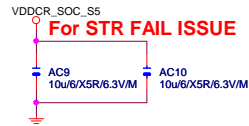
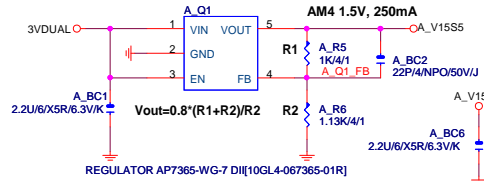
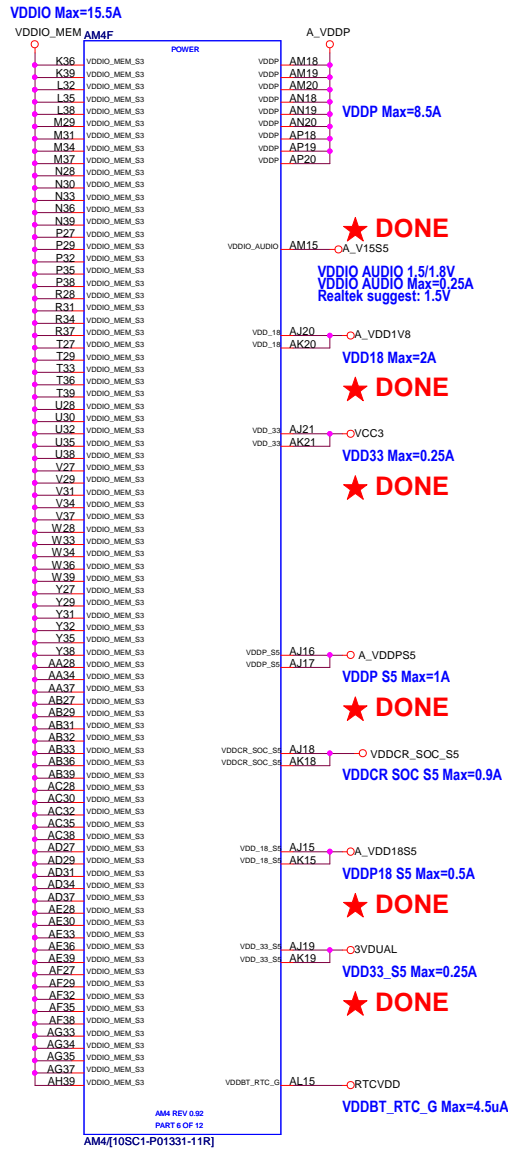
Title: **CPU CONTROL**

Size: Custom Document Number: **GA-AB350M-GAMING 3** Rev: **1.0**

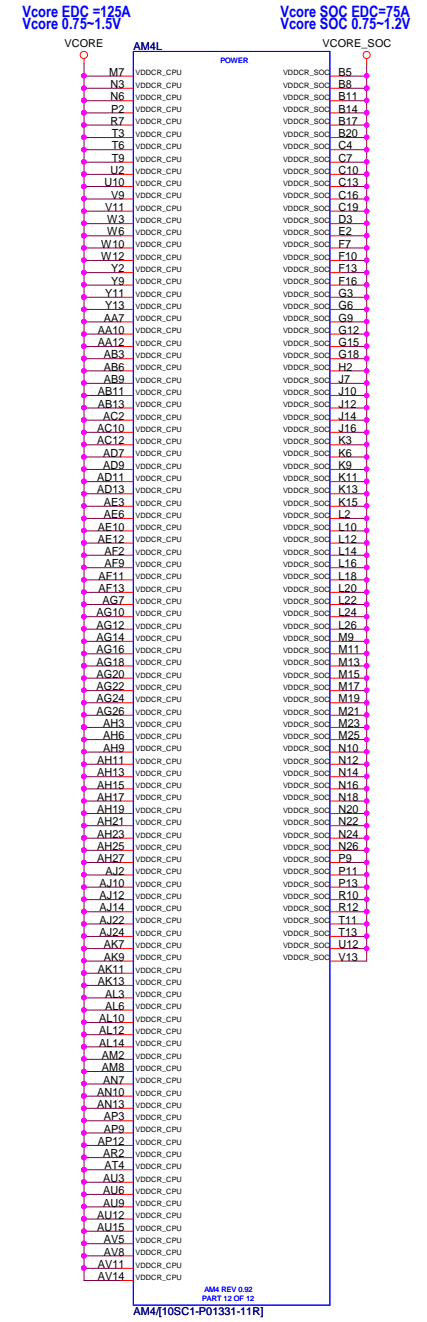
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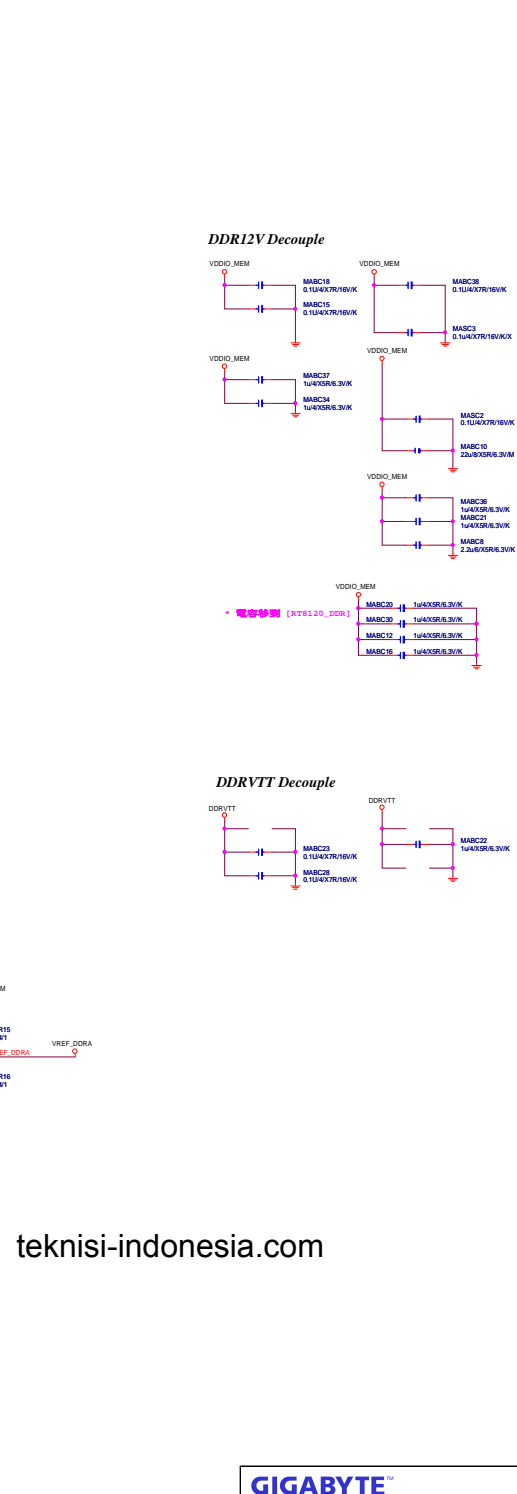
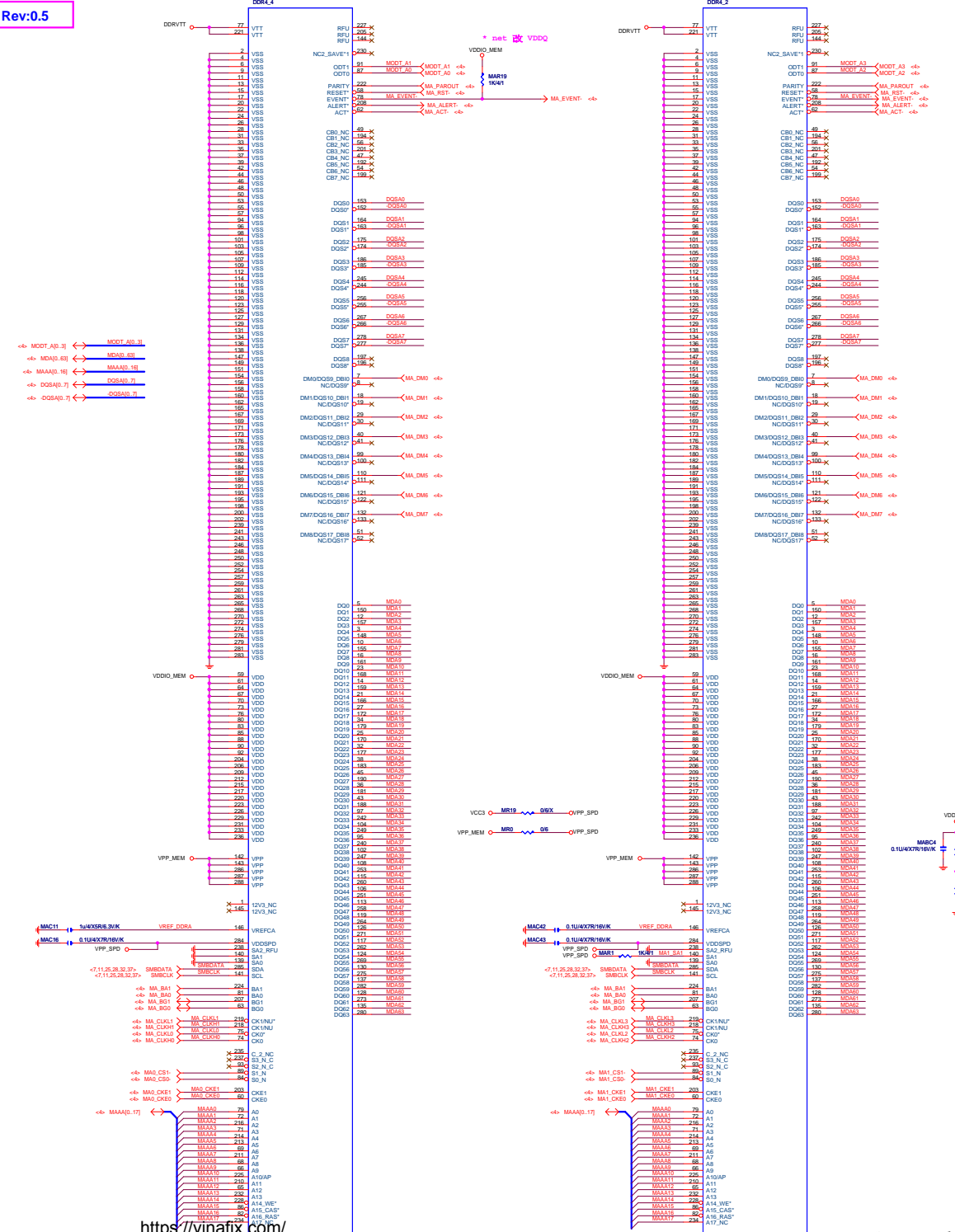


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	



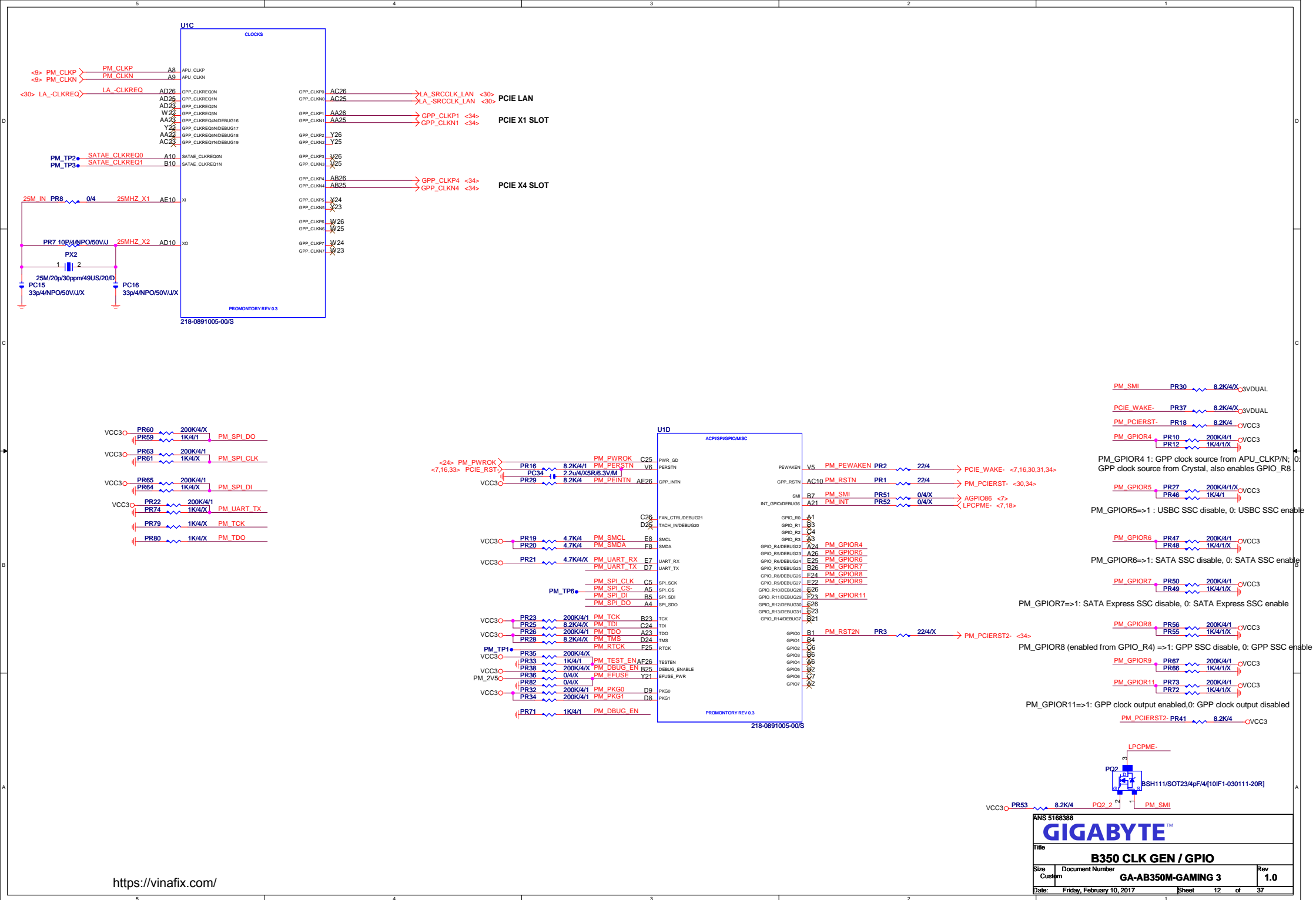
GIGABYTE™			
Title			
CPU POWER & GND			
Size	Document Number	Rev	
Custom	GA-AB350M-GAMING 3	1.0	
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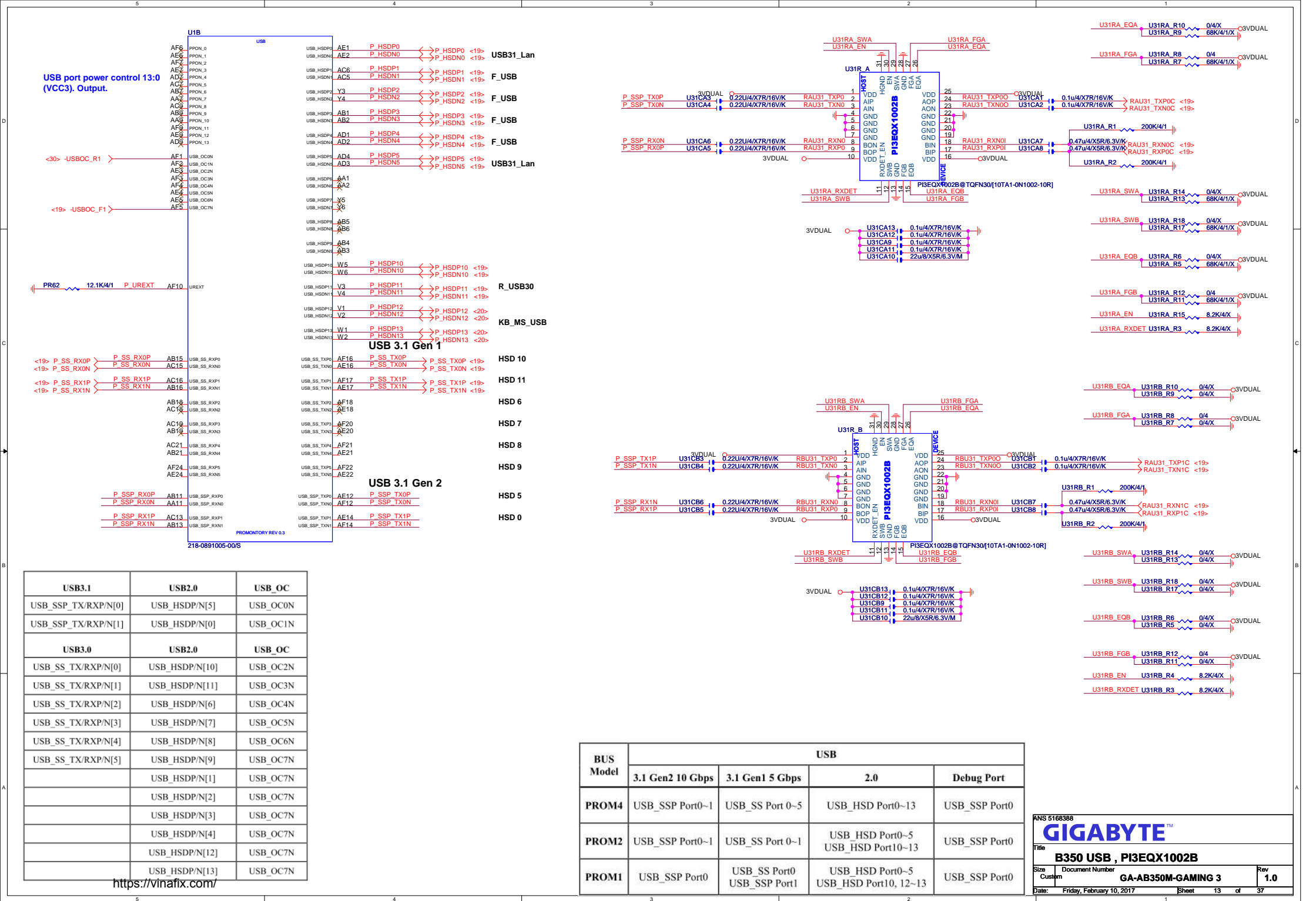
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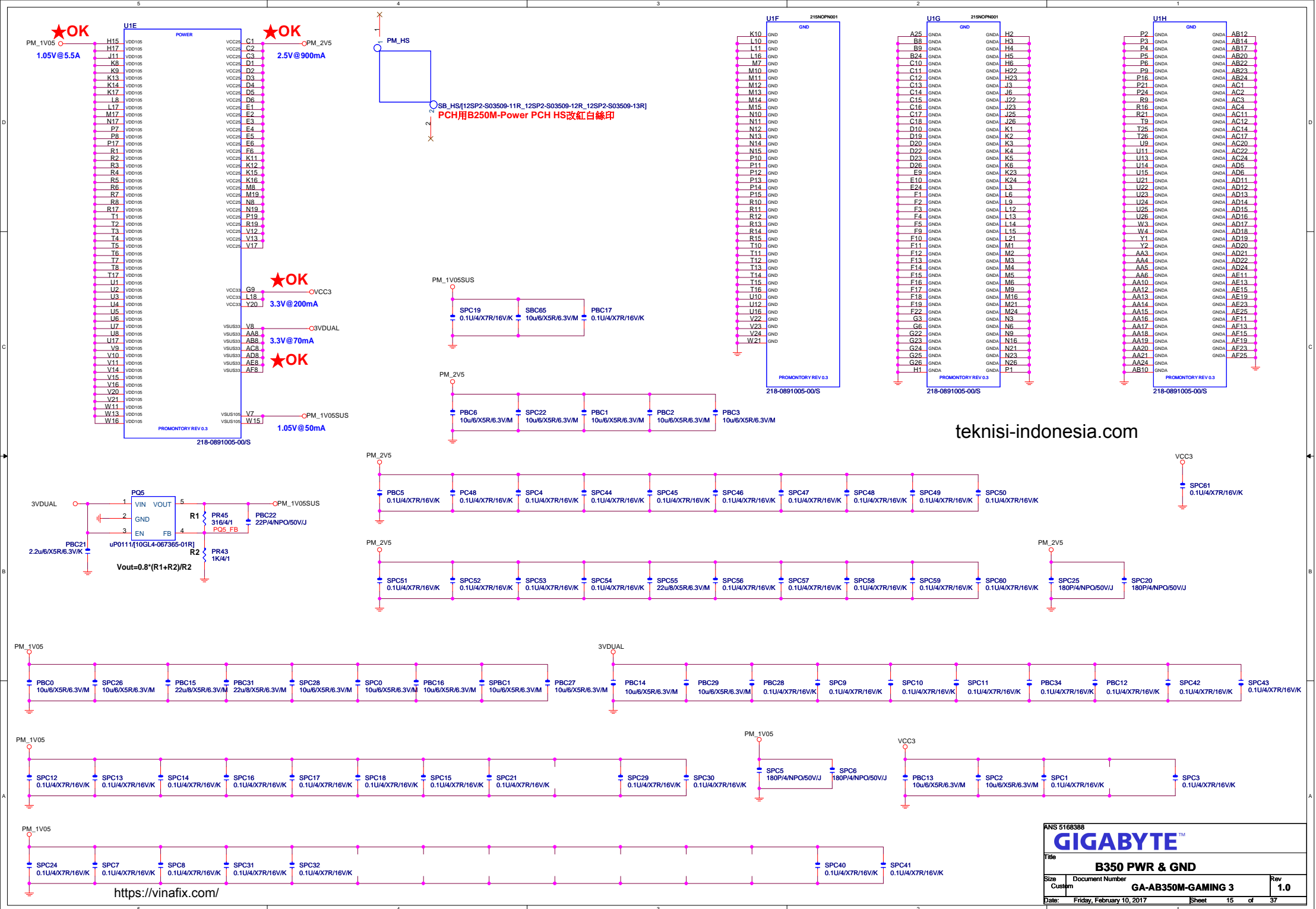


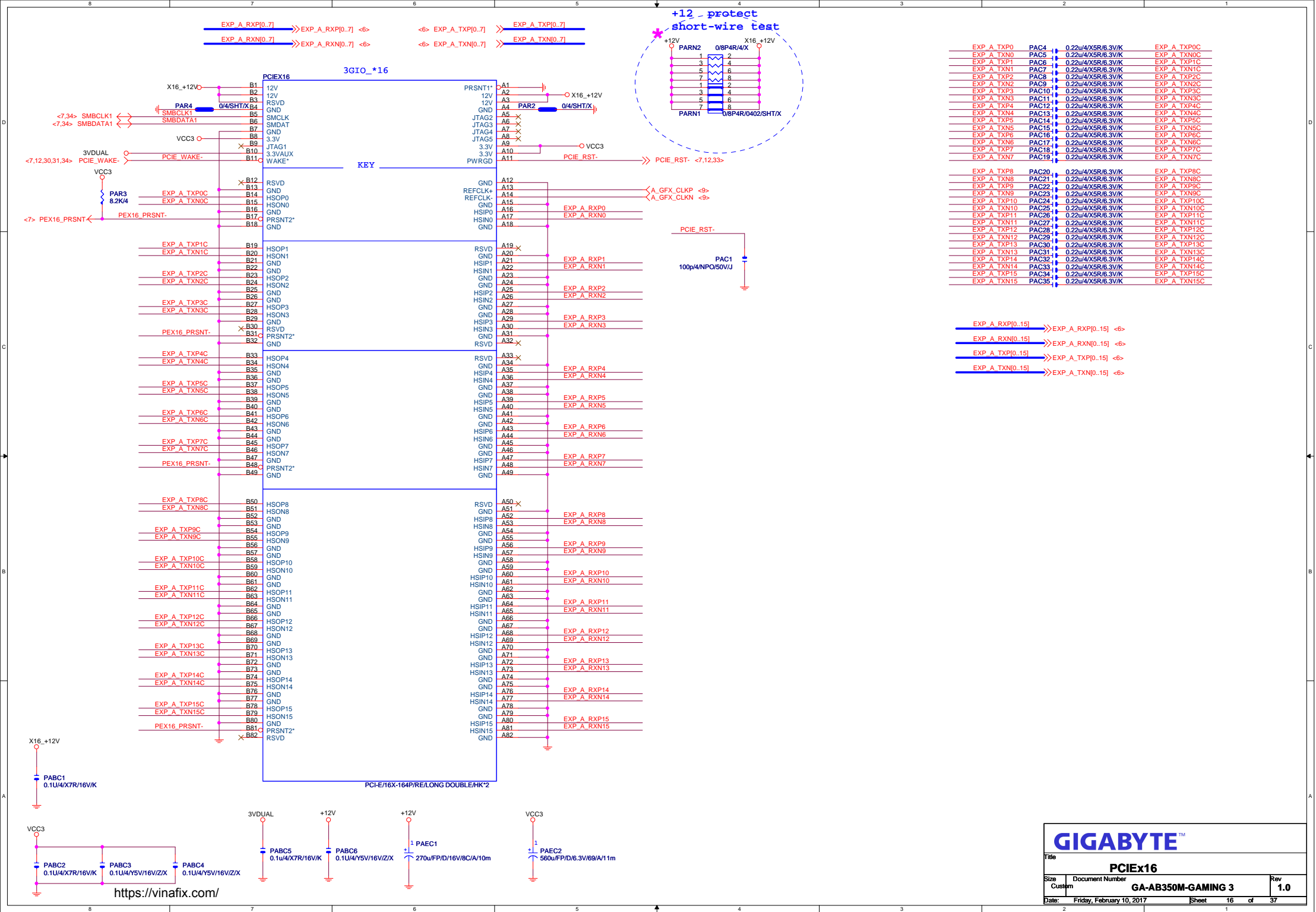
teknisi-indonesia.com

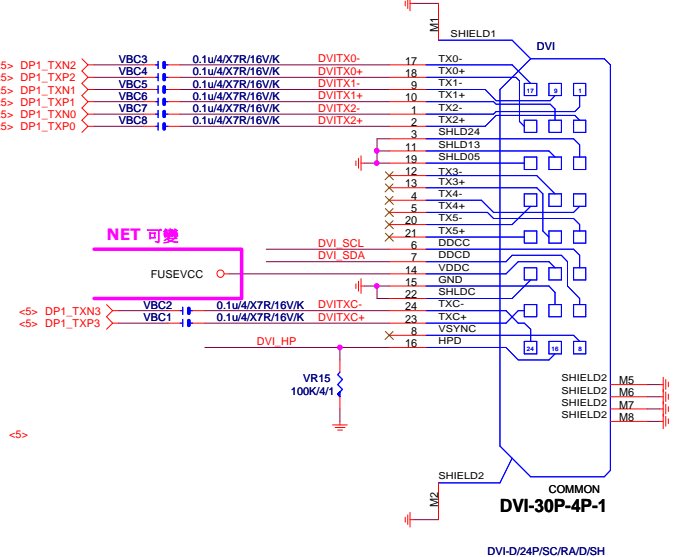
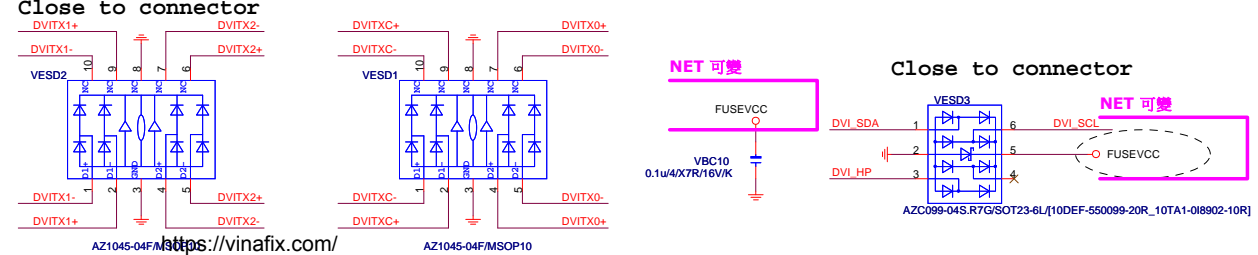
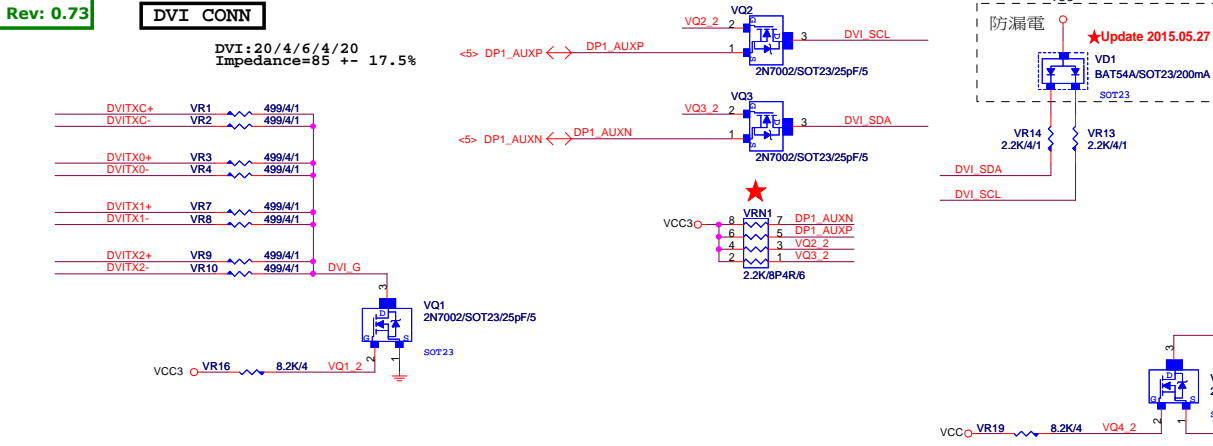
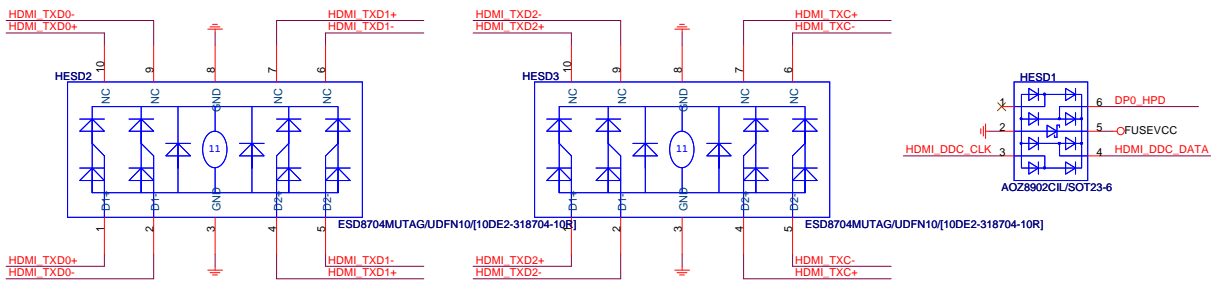
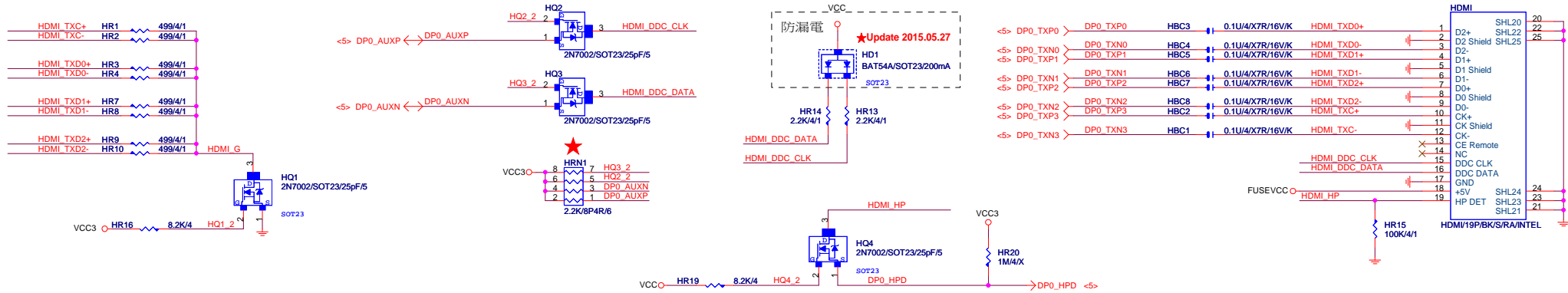
GIGABYTE		
DDR4 CHANNEL A		
File	Document Number	Rev
Size	GA-AB350M-GAMING 3	1.0
Combin		
Date	Friday, February 05, 2017	Page 10 of 37



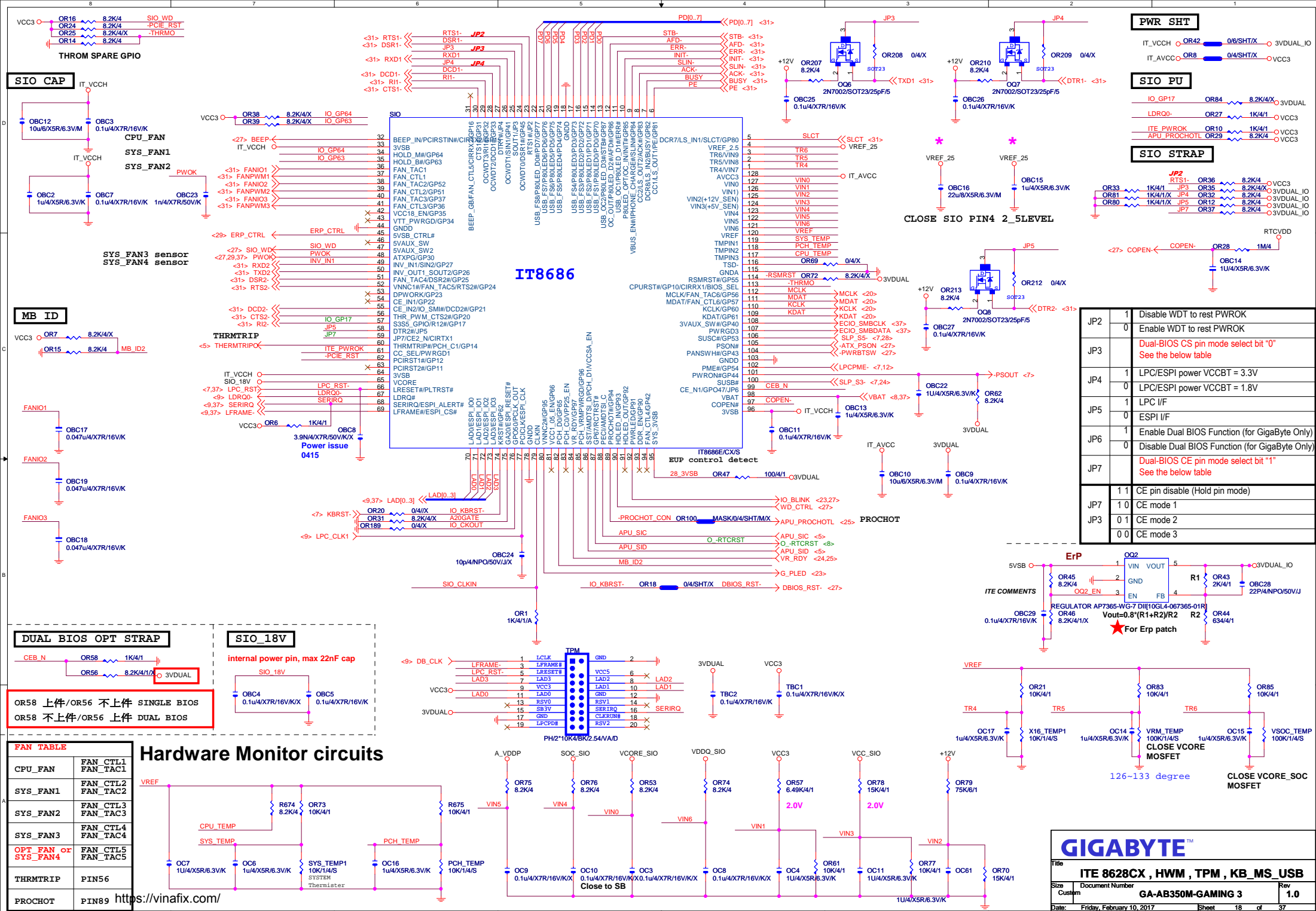








Title			HDMI, DVI
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JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

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ITE 8628CX , HWM , TPM , KB_MS_USB

Size Custom

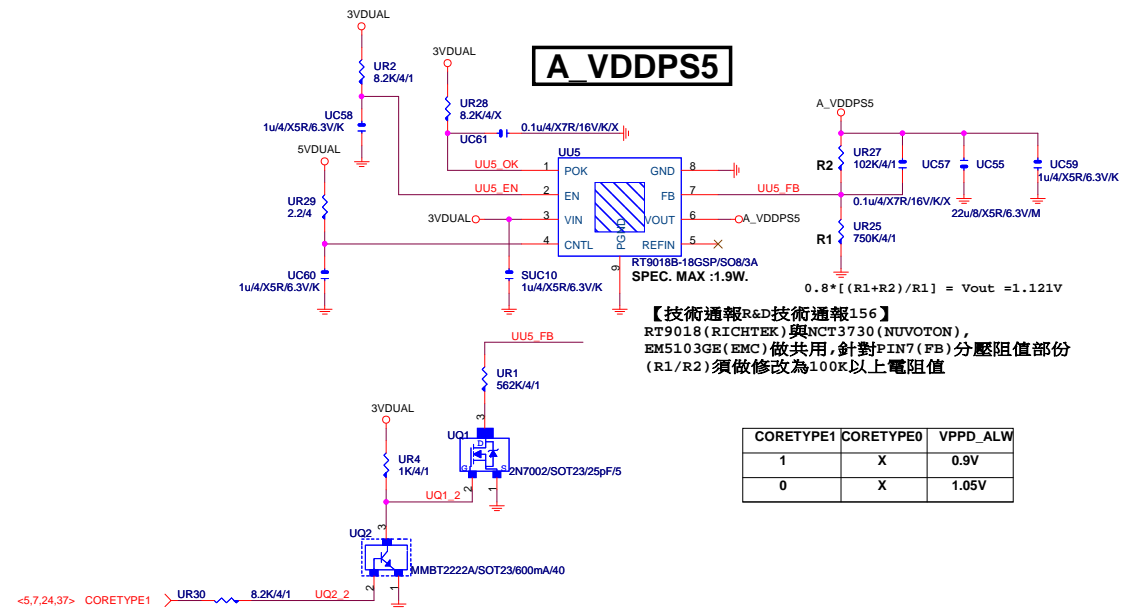
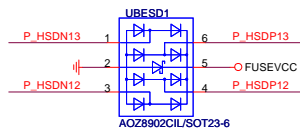
Document Number GA-AB350M-GAMING 3

Rev 1.0

Title

Date Friday, February 10, 2017

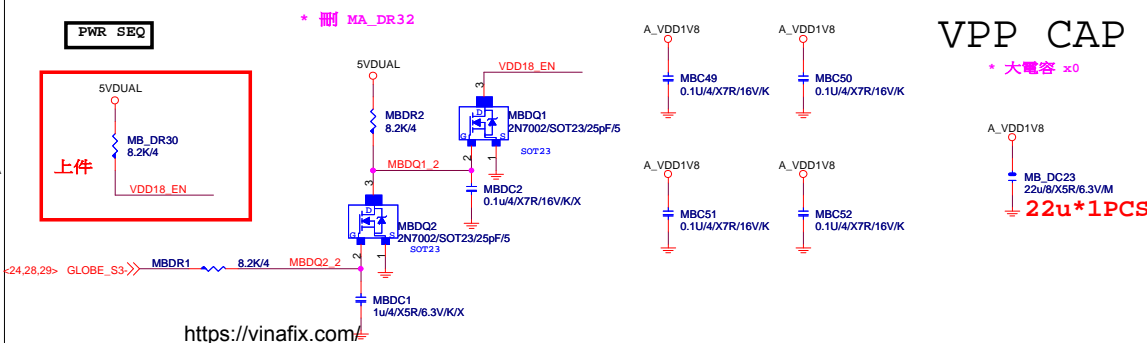
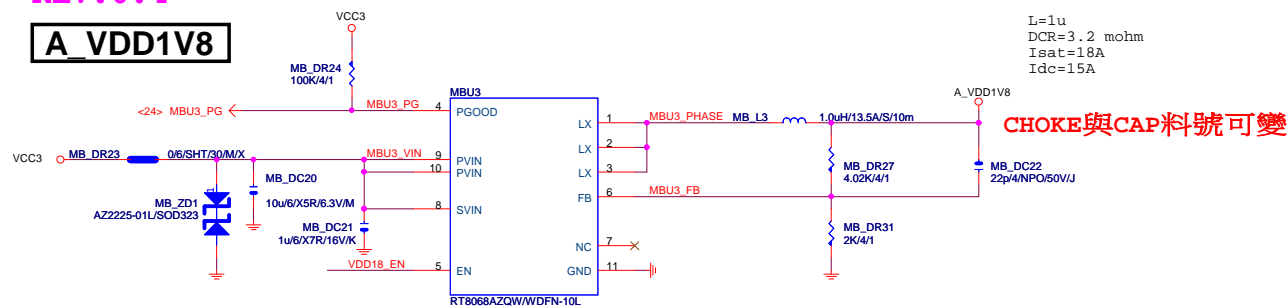
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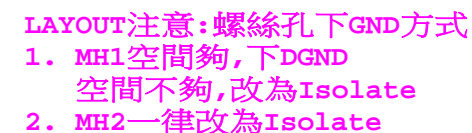


CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

REV: 0.4

A_VDD1V8





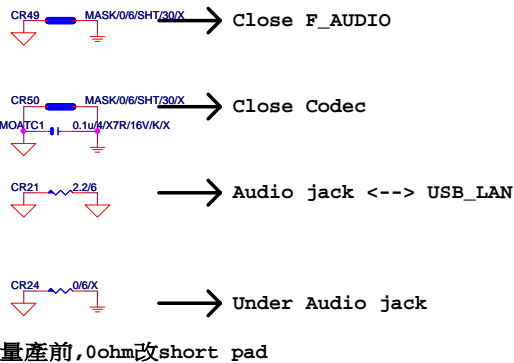
<input type="radio"/> MH1	<input type="radio"/> MH2	
DGND	Isolate	

GND切割線

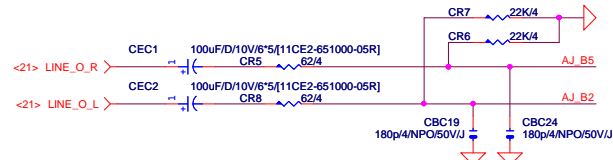


BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

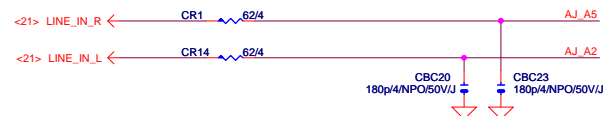
Rev 0.5



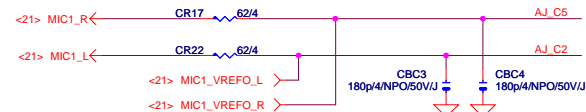
LINE-OUT



LINE-IN



MIC-IN



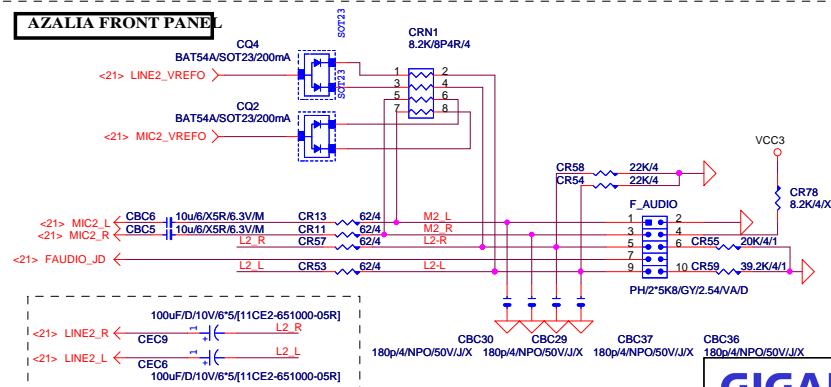
SURROUND

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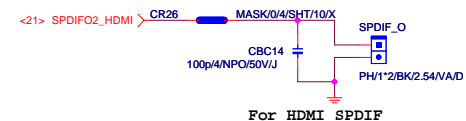
CEN/LFE

SURR BACK

AZALIA FRONT PANEL

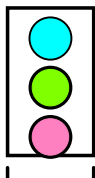


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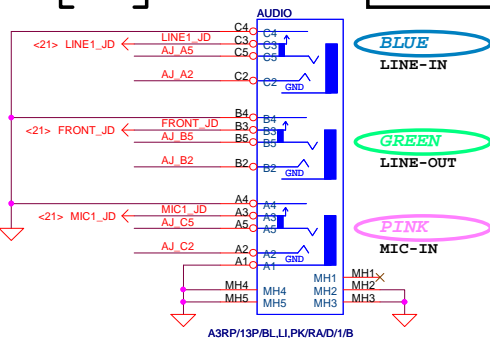


SPDIF_IN

AZALIA JACK



AZALIA JACK

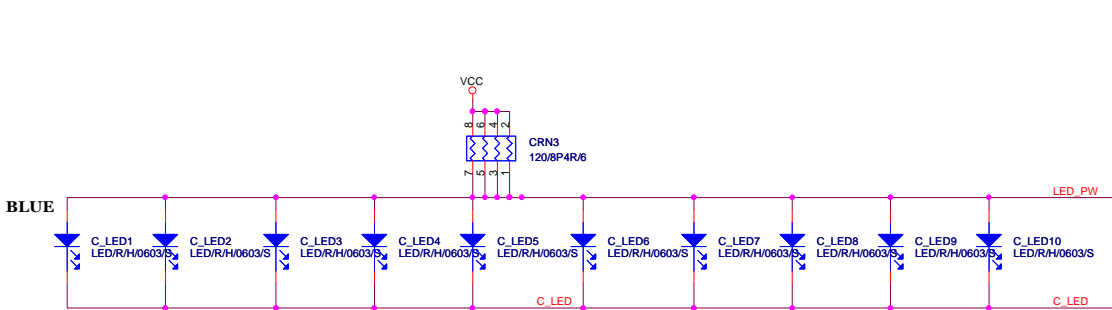


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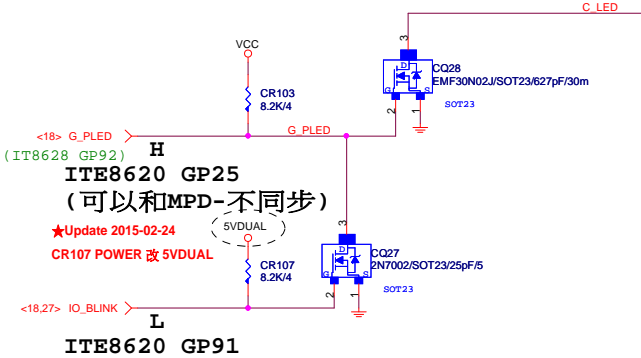
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AUDIO JACK		
Size	Document Number	Rev
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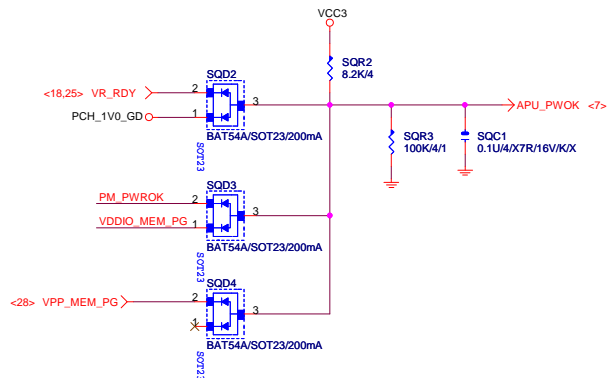
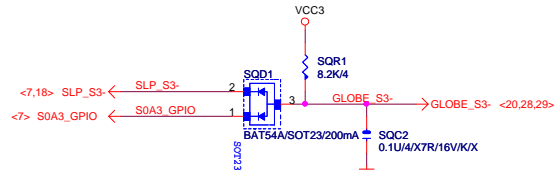
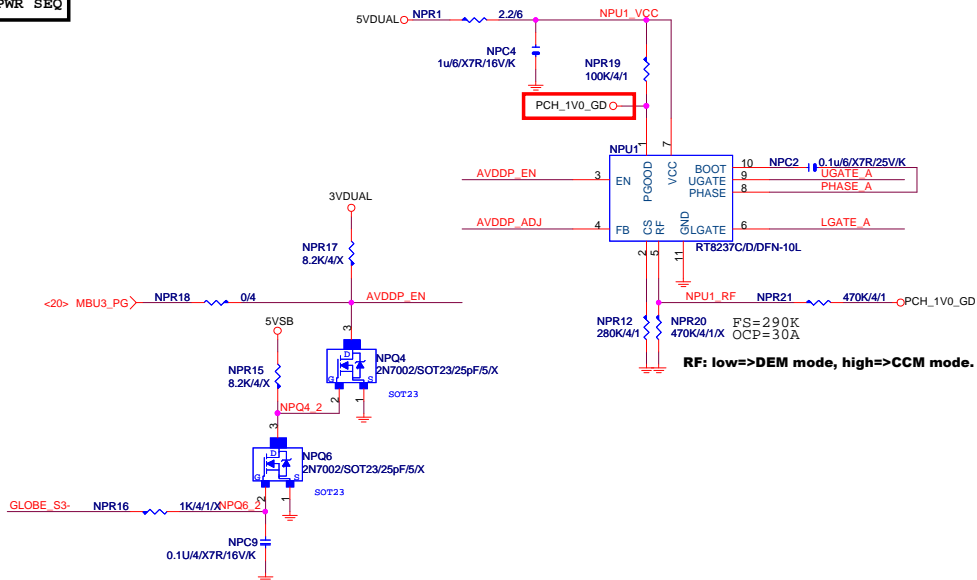
VALUE可變,LED顏色請自行修改
(預設:低亮度黃色LED:LED/Y/6/S)



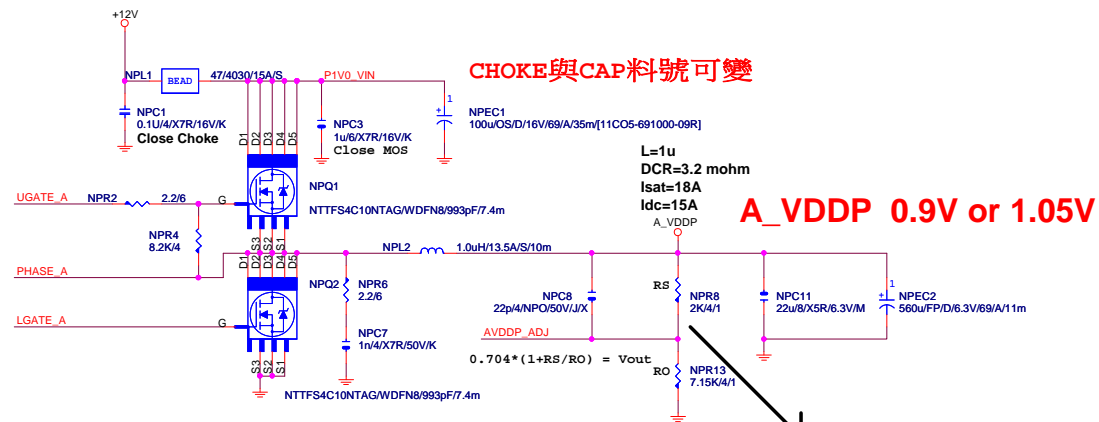
- BOM OPTION :
- 1. Chemicon音效電容
 - 2. 金屬外罩 Reserve (LAYOUT上件與否,依照各Model spec)
 - 3. LED Reserve (上件與否和LED顏色,依照各Model spec)

AUDIO LED Control			
	IO_GP25	IO_GP23	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

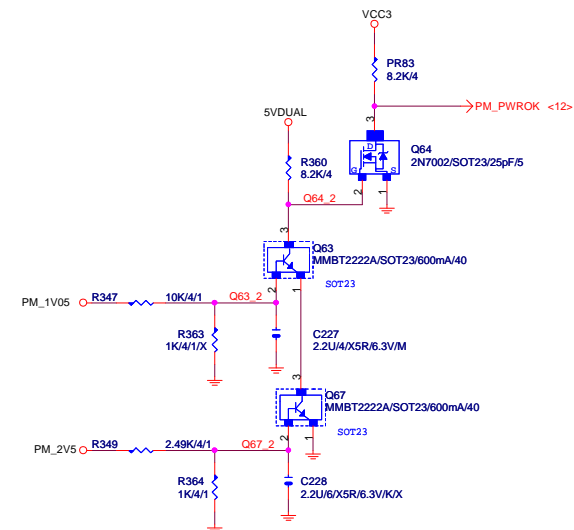
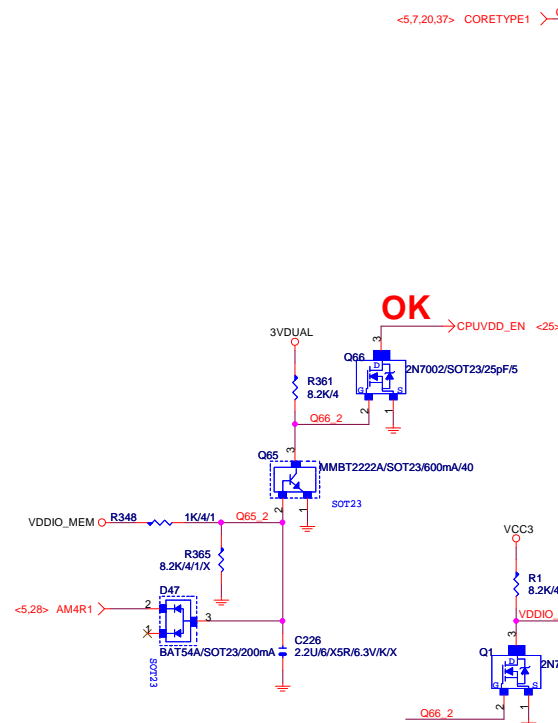




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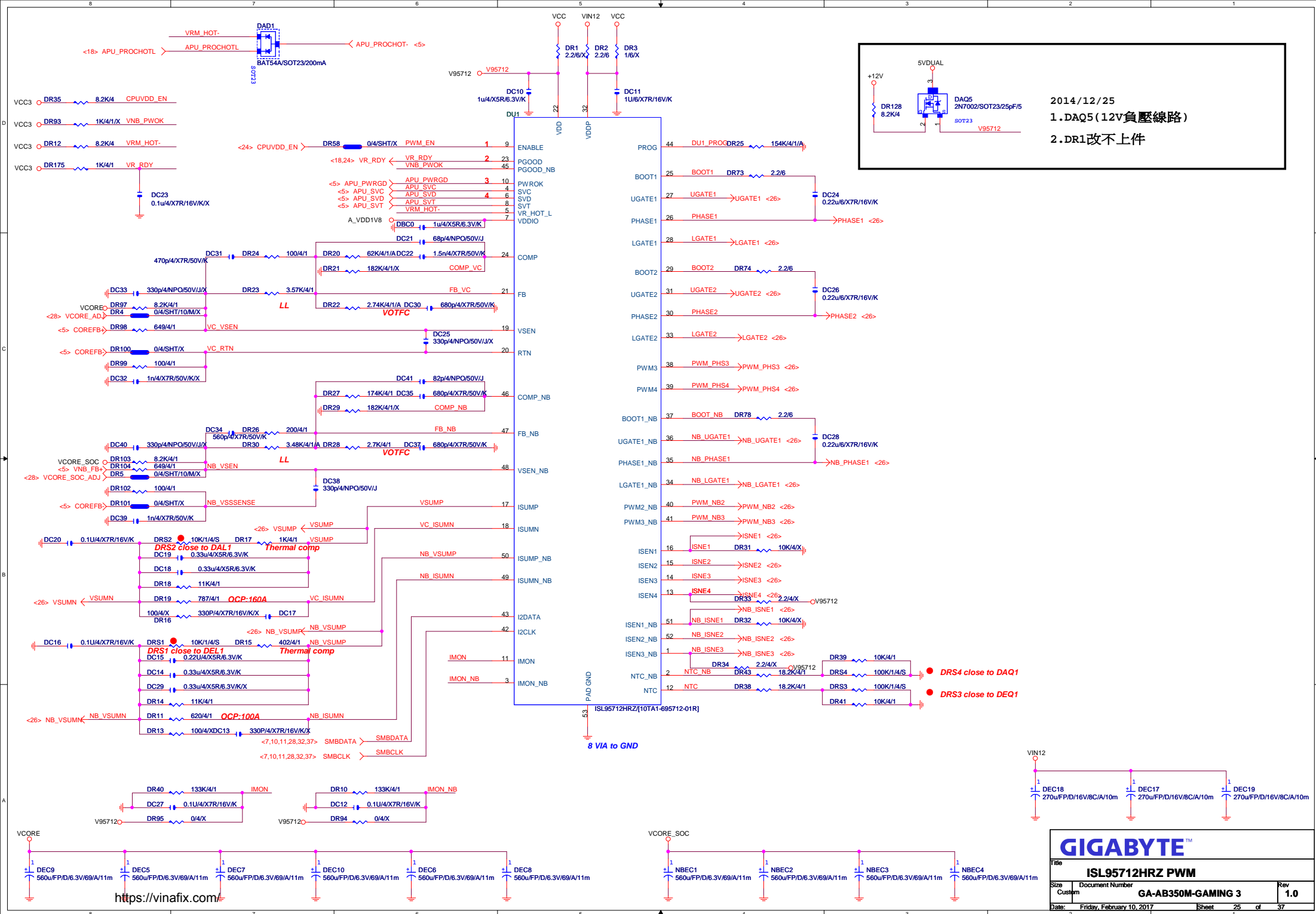


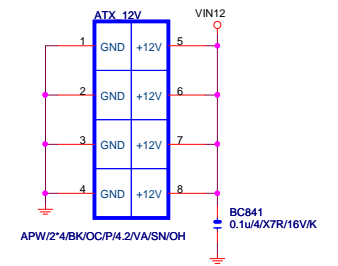
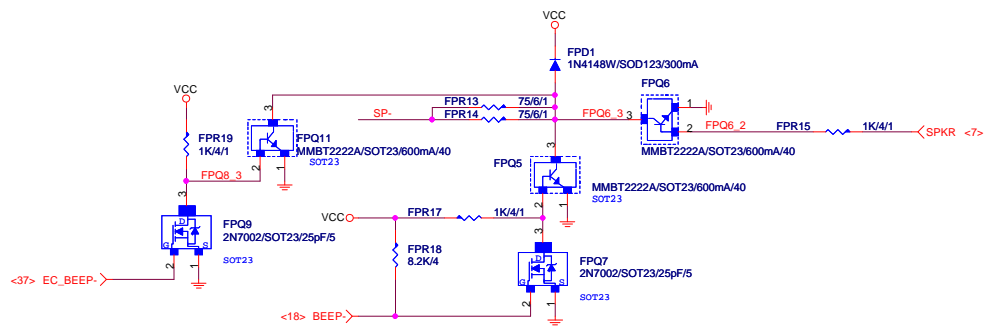
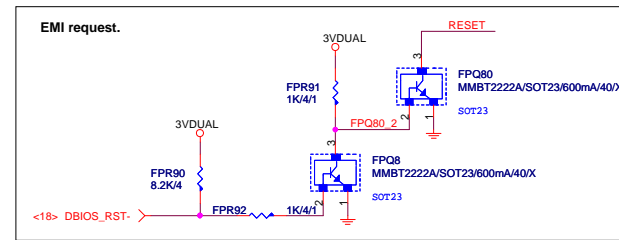
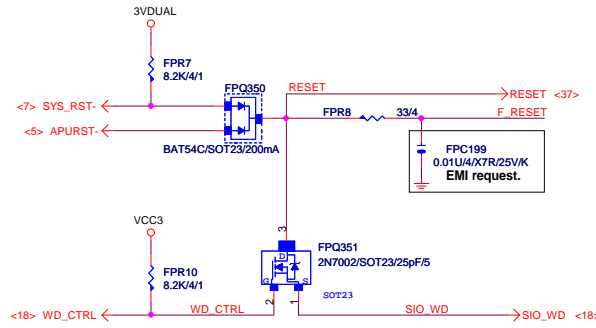
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V



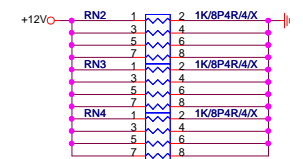
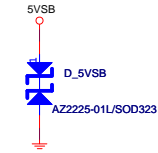
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POWER SEQUENCE		
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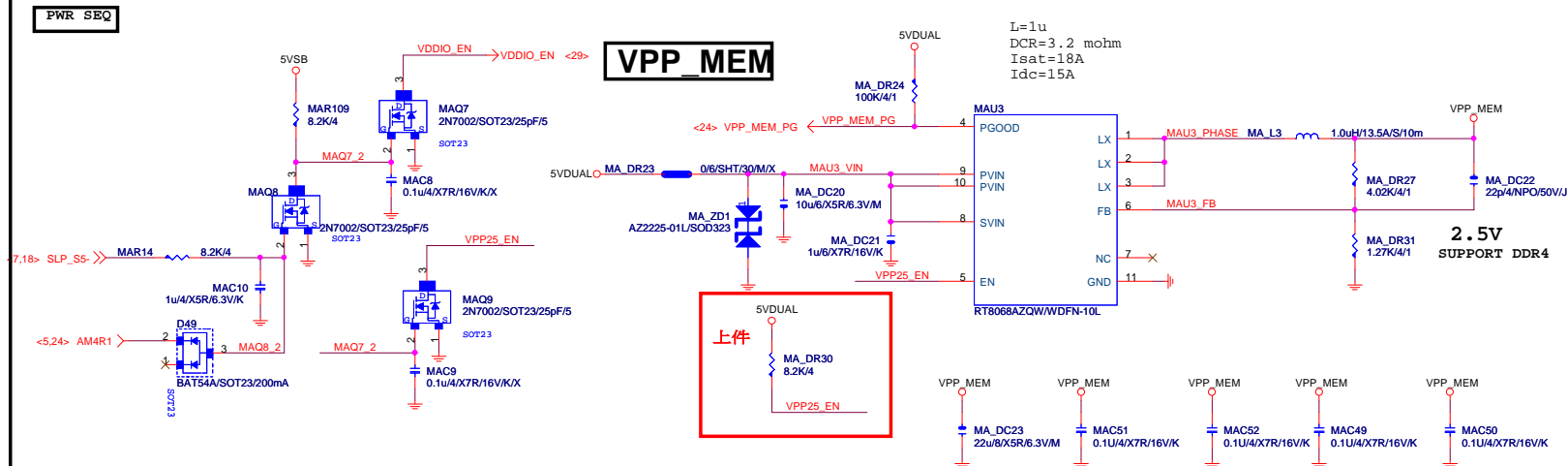
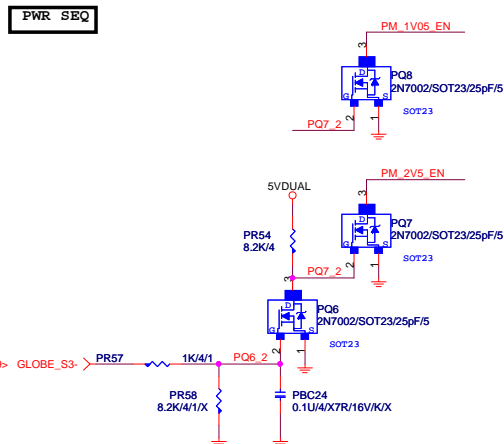
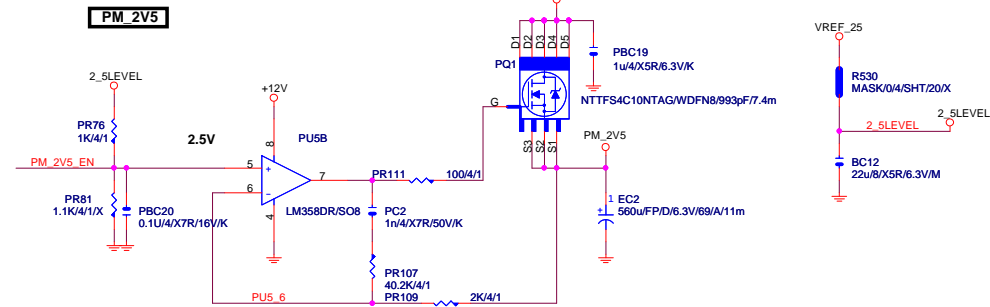
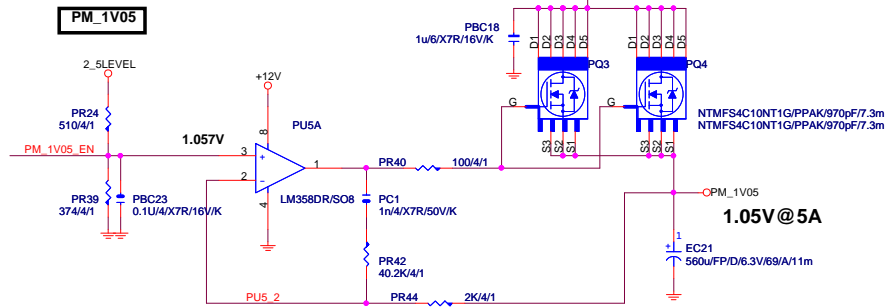




The diagram shows two channels, COUPON1 and COUPON2, with a transition from a high state to a low state. The transition is marked by a vertical line. The signal is labeled COUPON1, COUPON2, and COUPON/X. A 5V DUAL voltage level is indicated on the right.

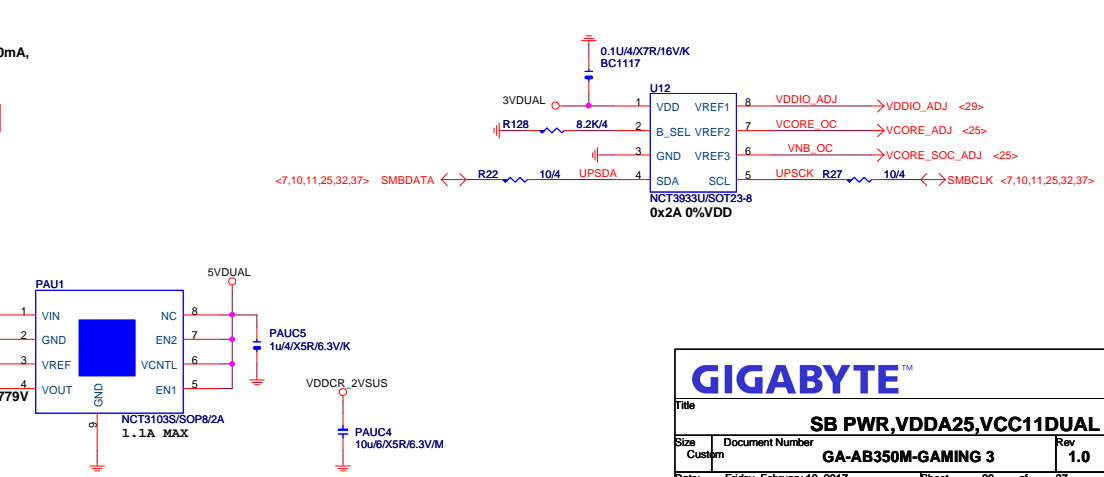
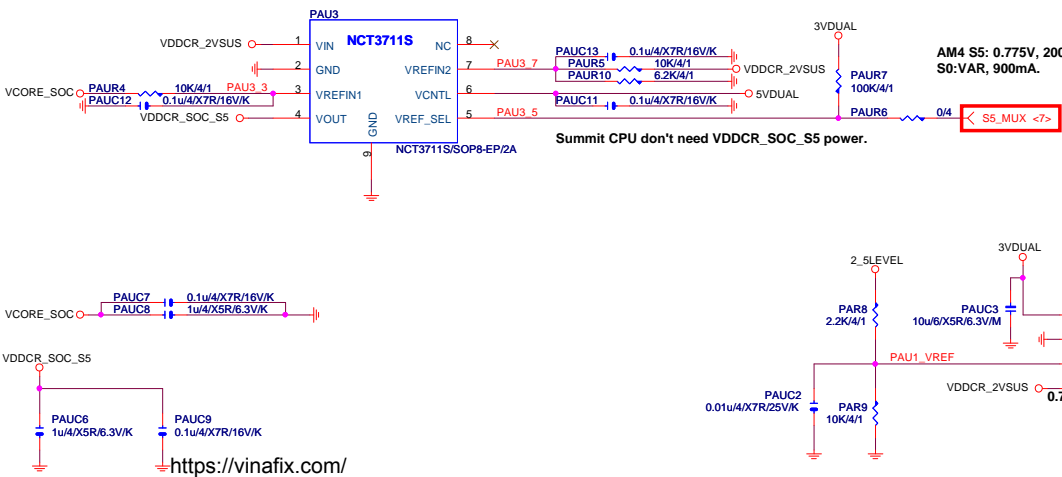


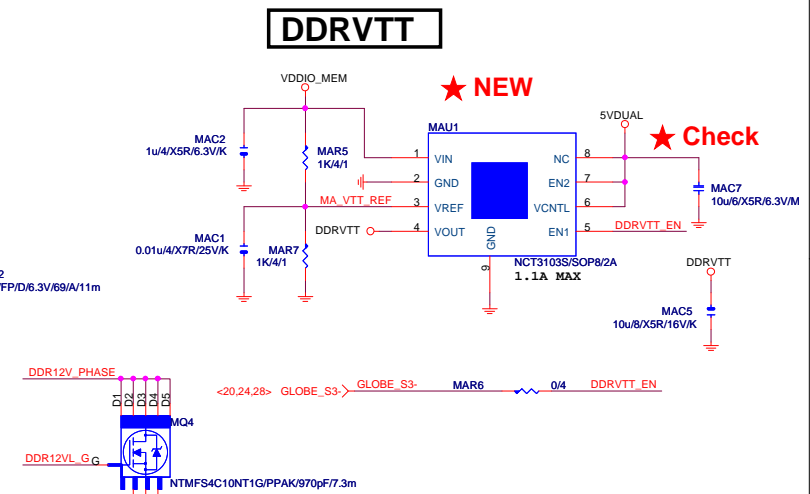
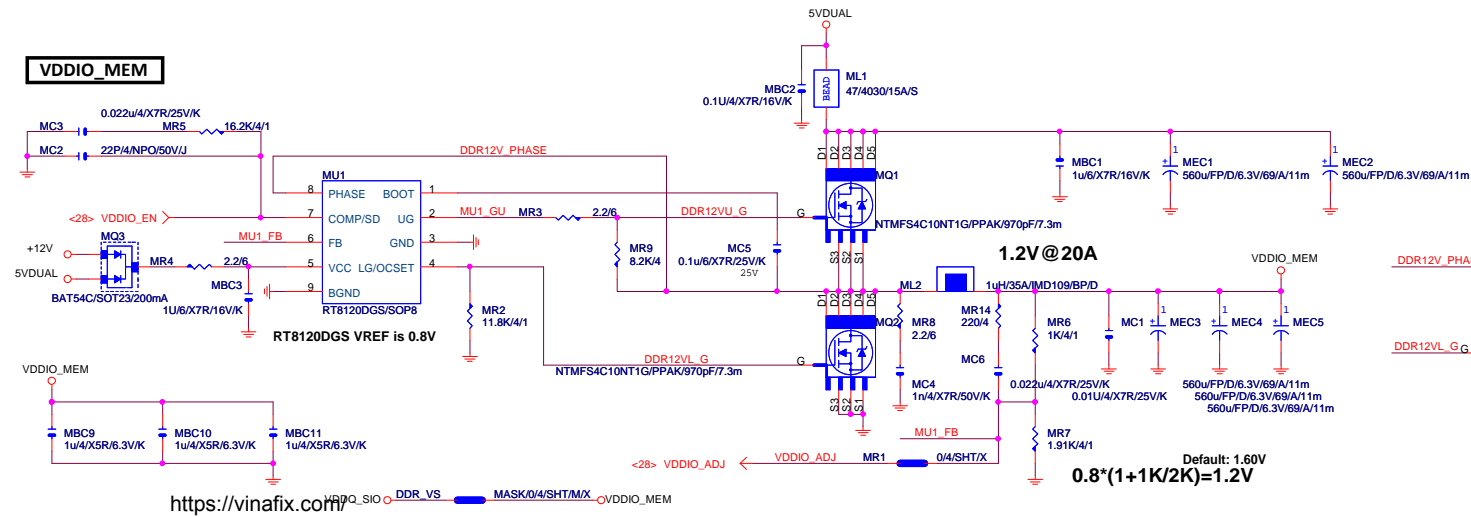
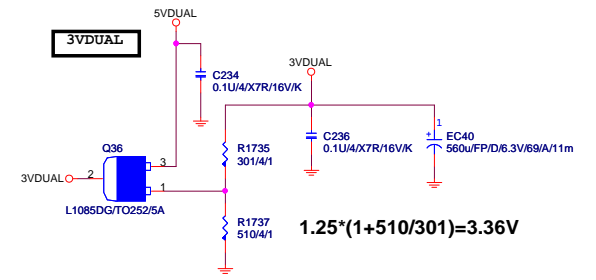
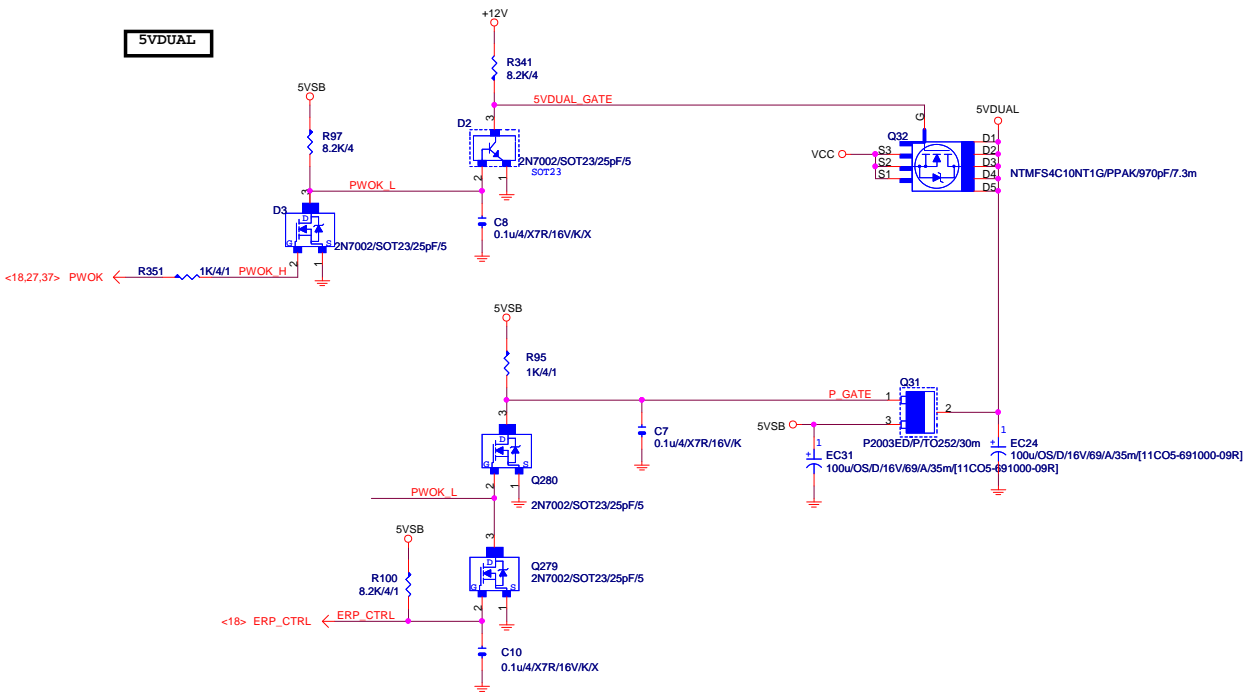
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Size	Document Number	Rev	
Custom	GA-AB350M-GAMING 3	1.0	
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VDDCR SOC S5

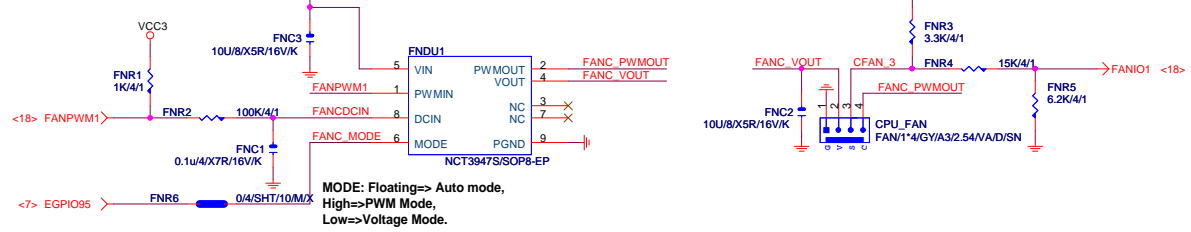
S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.



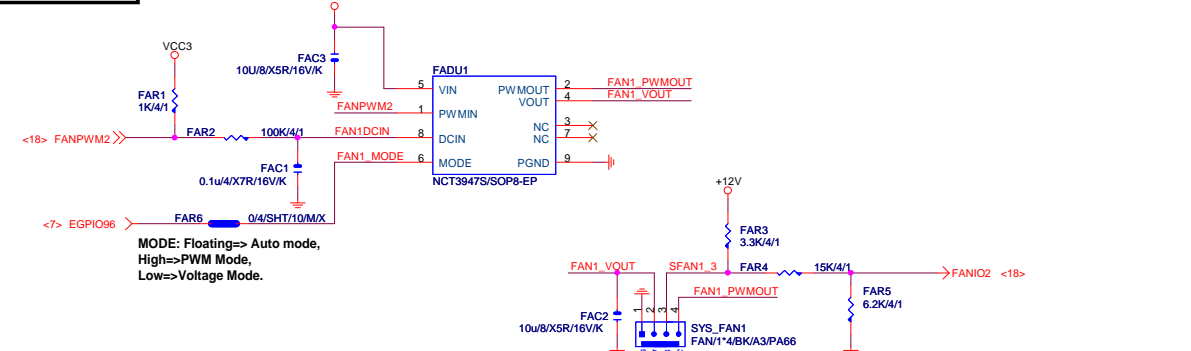


GIGABYTE™		
Title		
DDR PWR, 5VDUAL, ERP		
Size	Document Number	Rev
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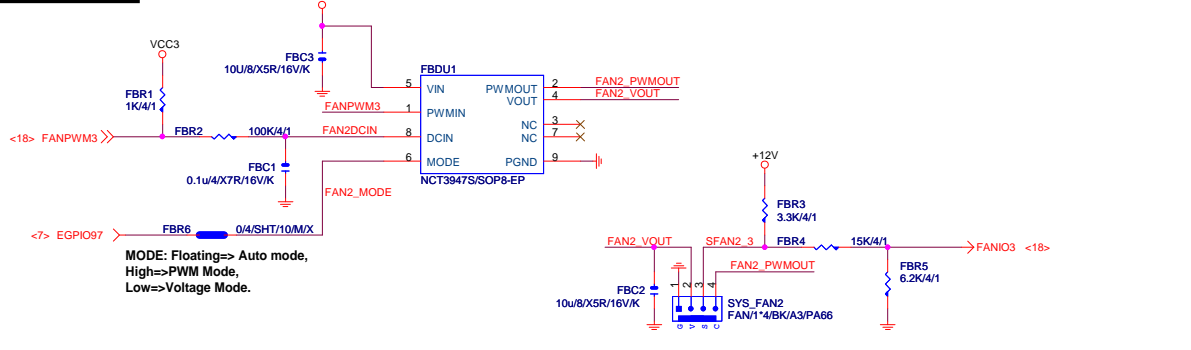
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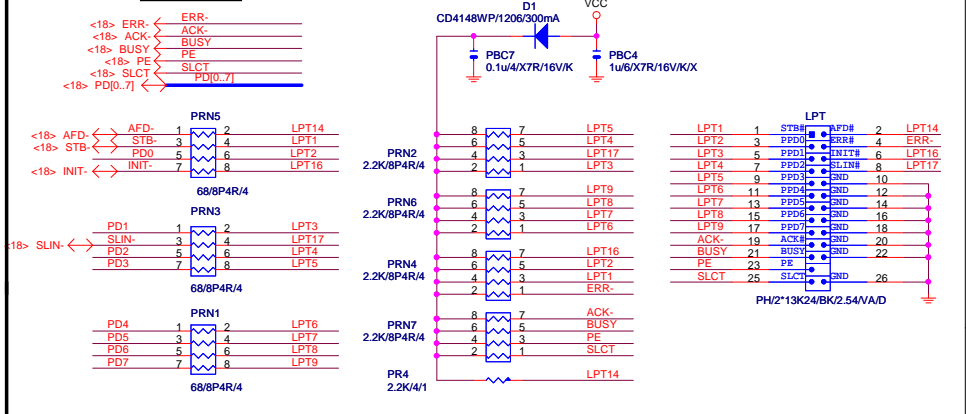
SYSTEM FAN1



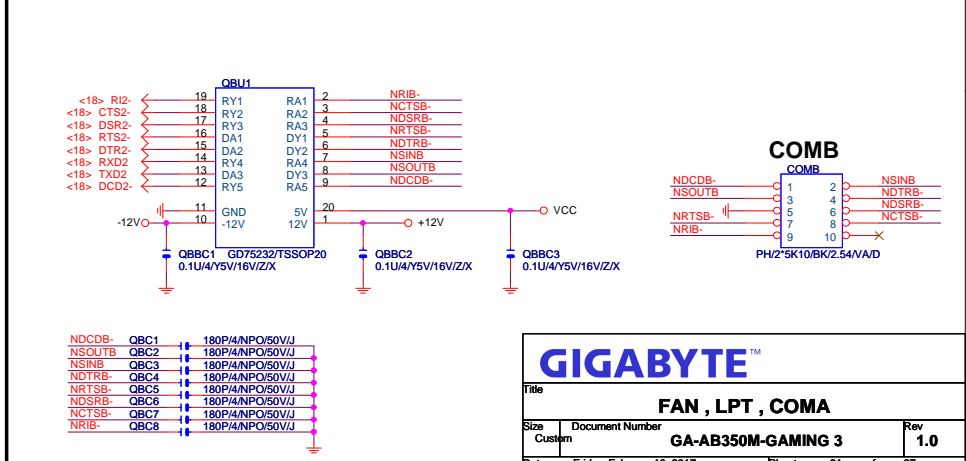
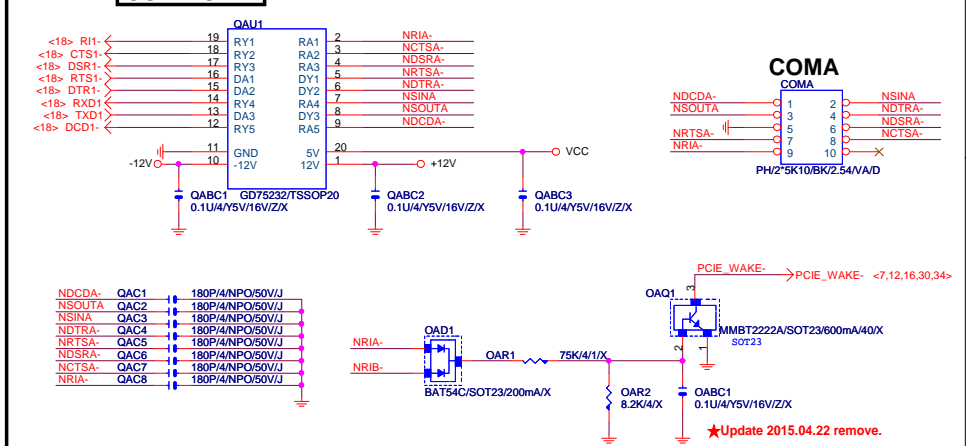
SYSTEM FAN2

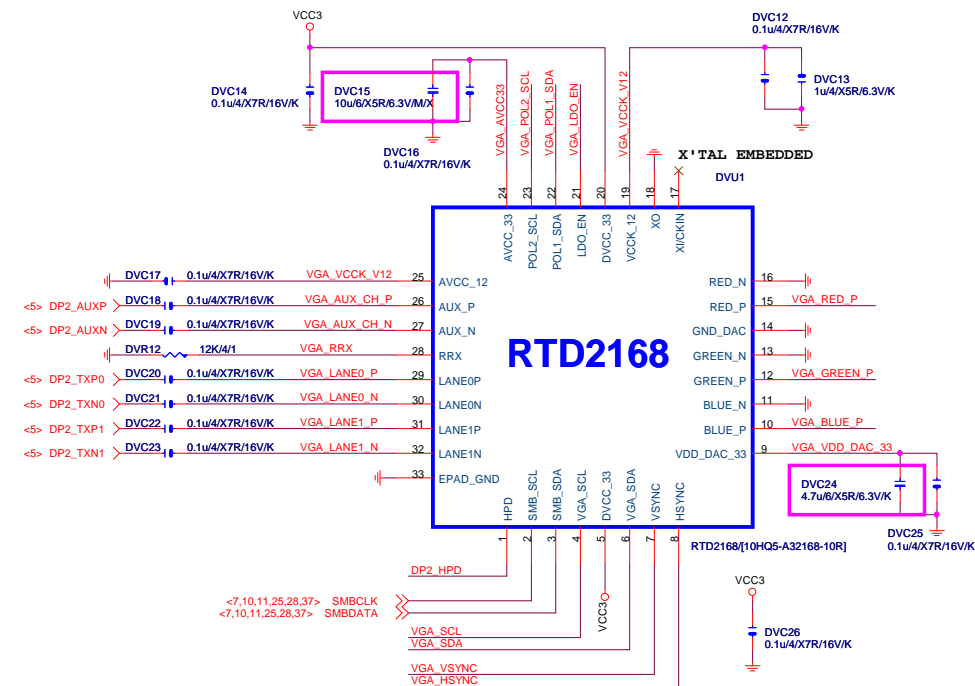


LPT PORT

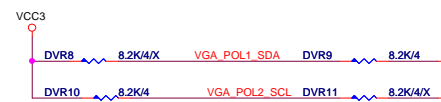


COM PORT



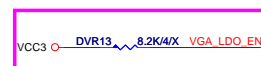


Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

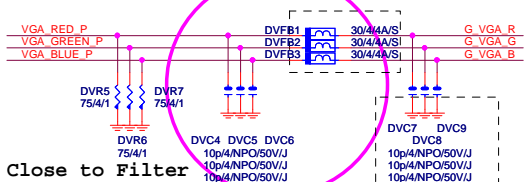
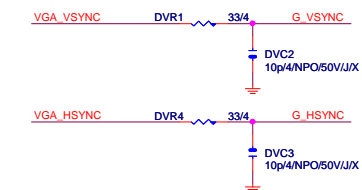


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD



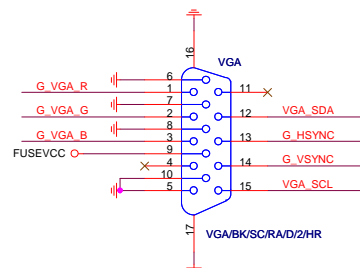
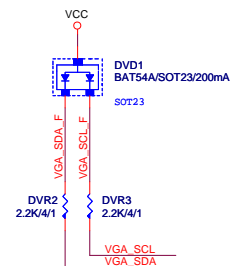
Gigabyte Technology



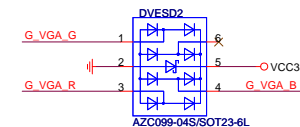
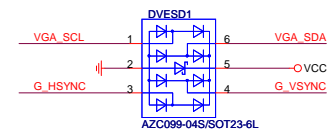
Close to Filter

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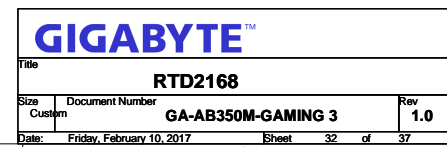
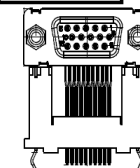
FOR EMI

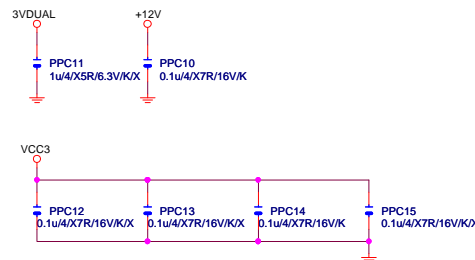
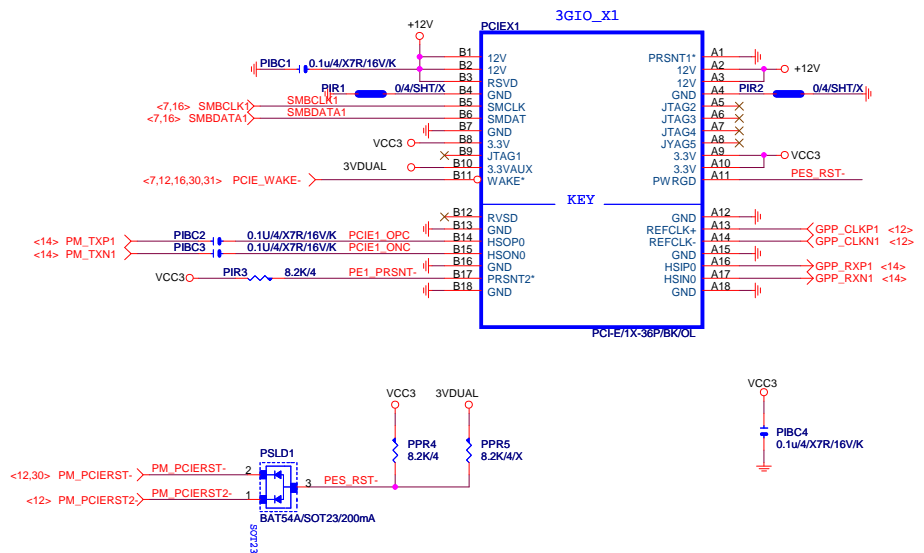
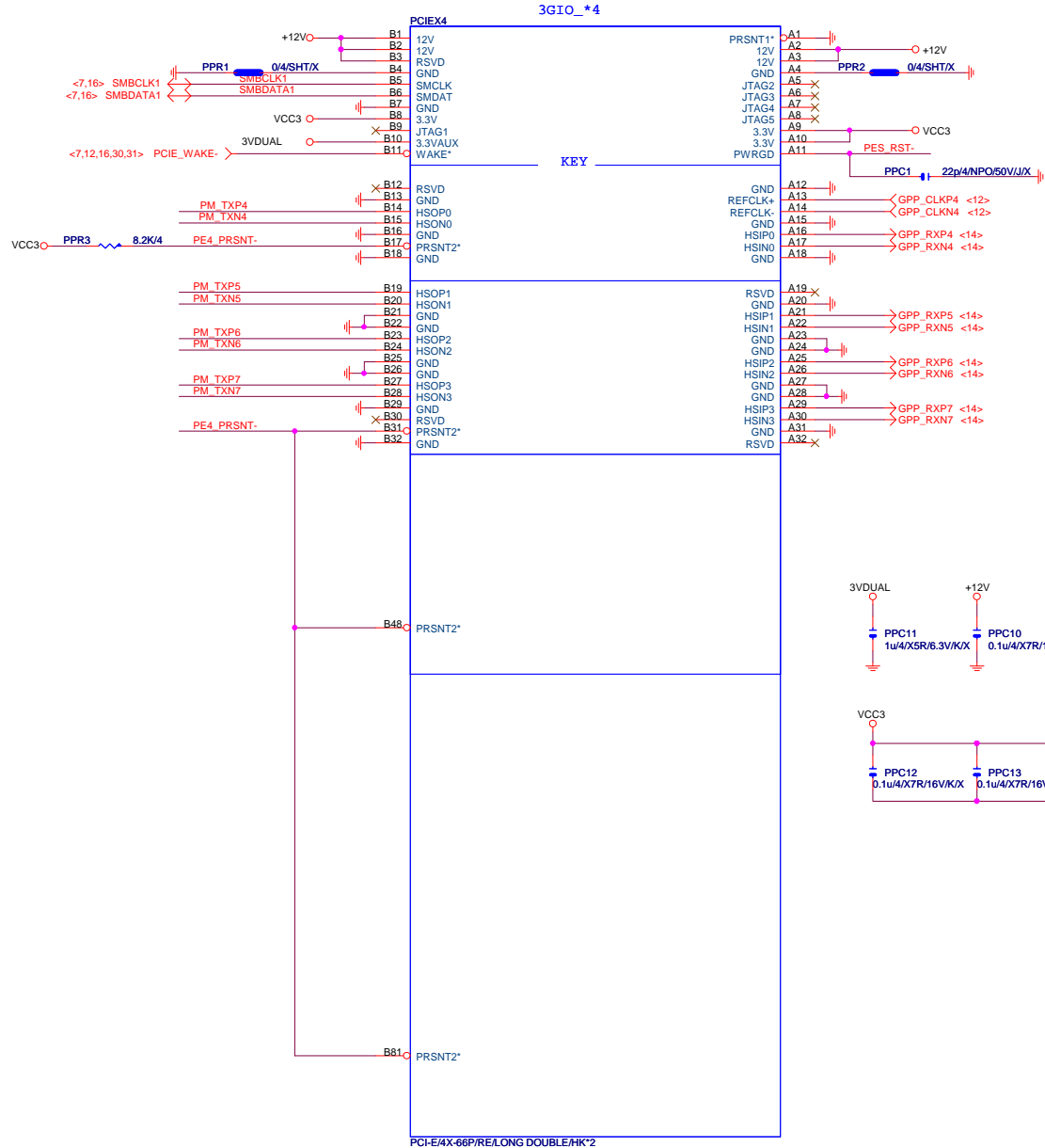


VGA ESD



VGA CONN. 架高型VGA (BLACK)



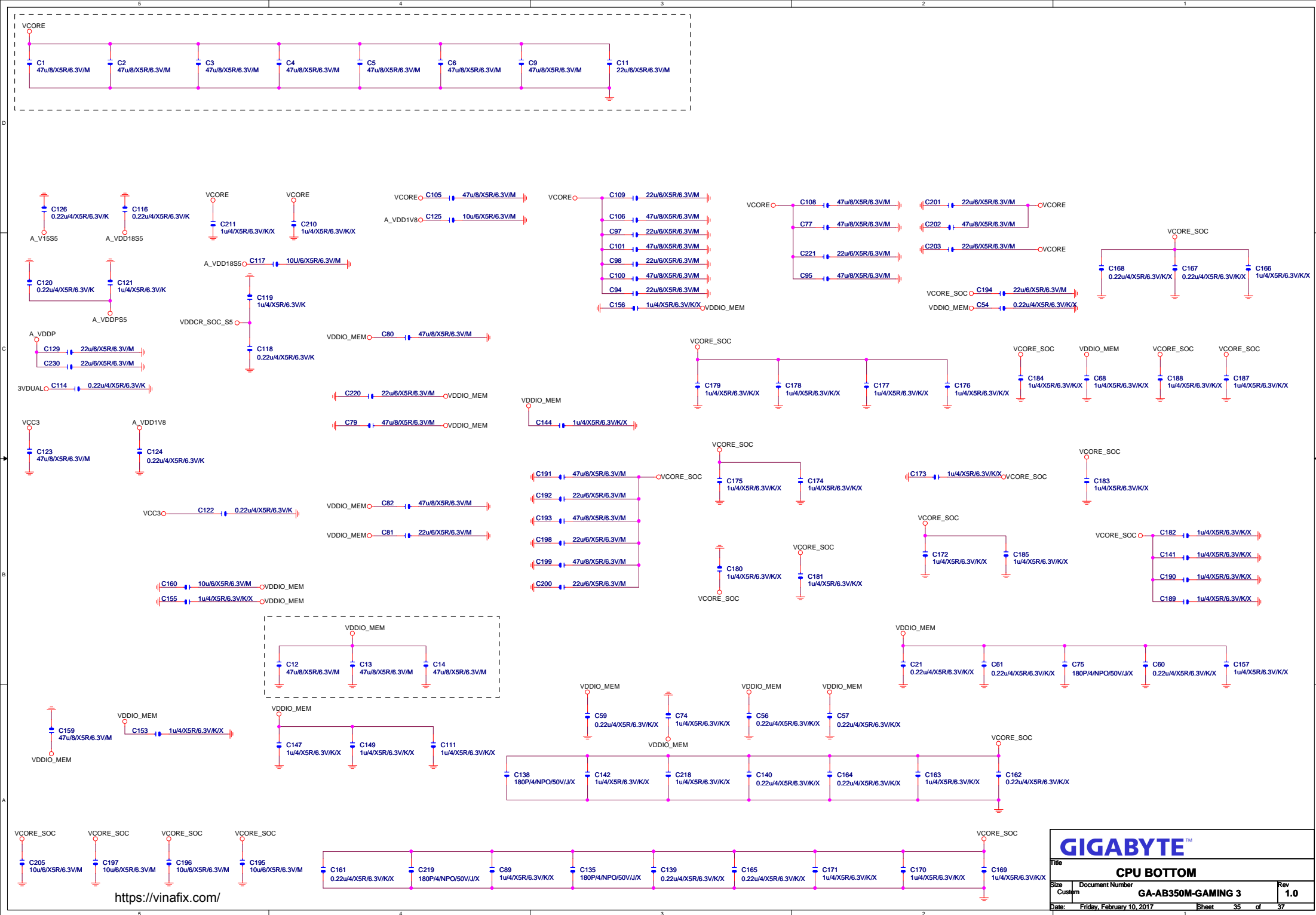


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<14> GPP_TXP4	GPP_TXP4	PPC2	0.1u/4/X7R/16V/K	PM_TXP4
<14> GPP_TXN4	GPP_TXN4	PPC3	0.1u/4/X7R/16V/K	PM_TXN4
<14> GPP_TXP5	GPP_TXP5	PPC4	0.1u/4/X7R/16V/K	PM_TXP5
<14> GPP_TXN5	GPP_TXN5	PPC5	0.1u/4/X7R/16V/K	PM_TXN5
<14> GPP_TXP6	GPP_TXP6	PPC6	0.1u/4/X7R/16V/K	PM_TXP6
<14> GPP_TXN6	GPP_TXN6	PPC7	0.1u/4/X7R/16V/K	PM_TXN6
<14> GPP_TXP7	GPP_TXP7	PPC8	0.1u/4/X7R/16V/K	PM_TXP7
<14> GPP_TXN7	GPP_TXN7	PPC9	0.1u/4/X7R/16V/K	PM_TXN7

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GIGABYTE™			
Title			
PCIEx4 , PCIEx1			
Size	Document Number	Rev	
Custom	GA-AB350M-GAMING 3	1.0	
Date:	Friday, February 10, 2017	Sheet	34 of 37



CPU TOP CAVITY

